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Electronics, Photonics, Microsystems

Tomasz Fałat, Jan Felba, Przemysław Matkowski

PACKAGING OF ELECTRONICS, PHOTONICS AND MICROSYSTEMS

Wrocław 2011

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1. Introduction

The electronic product is like a human body. Electronic products have “brains” or microprocessors, and their packaging provides the “nervous” and “skeletal” systems. Therefore, note that without *packaging*, an electronic system is useless. It needs its packaging in order to be interconnected, powered or “fed”, cooled via its “circulatory” system, and protected via its “skeletal” system. There are other similarities such as the electrical and mechanical transducers to those in the body, and photodiode functions as the human eye. At the current IC integration rate following Moore's Law, it will be the year 2020 before the computer memory and processing technology catches up with the human brain [1].

The functions of an electronic package are to protect, power and cool the microelectronic chips or components and provide electrical and mechanical connection between the microelectronic part and the outside word. Whether a single transistor or a gigascale integration (GSI) chip, they have to be packaged. As such, the electronic package is an integral part of the microelectronic system. The challenge for the package is to provide all crucial functions required by the microelectronic part without limiting the performance of the part. To meet this challenge, the package technology has also evolved from a simple metal can to very complex multilayer ceramic and organic structures. But as the semiconductor technology progresses towards higher levels of integration, high performance and increasing functionality, the design and fabrication of the package that will meet the requirements of modern and future microelectronic systems becomes increasingly complex and challenging [2].

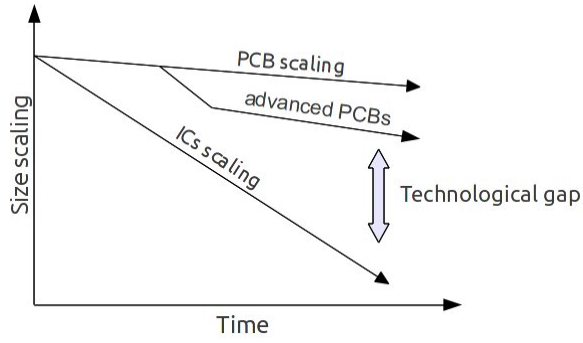


Figure 1.1 The differences between ICs scaling and possibility of standard electronics interconnecting technologies

One of the most critical levels of electronic packaging is that of packaging and interconnecting integrated circuits (ICs) and semiconductor devices. These elements are the heart and control of electronic systems, and since they are typically sensitive to electrical, mechanical, physical, and chemical influences, they require special considerations by the packaging engineer. Packaging is the middle link of the process that produces these systems. Hence, it must respond to demands from both ends, that is, wafer fabrication and device trends upstream (circuit level) and circuit board assembly and systems performance trends downstream (system level). This is particularly true in the design, assembly, interconnection, and fabrication aspects of IC packaging. Today circuit and system level demands, many contradictory, are forcing the packaging engineer to make changes in packaging methods at a time when requirements for performance, in particular for reliability, are at their most severe. Many electronic system performance problems result from a lack of knowledge and understanding of the many interfacing parameters at this level of packaging.

Packaging engineers must be aware of these industry demands and trends to address the technical and business needs of the near future [3].

One of the most dominant trend in microelectronic development is miniaturization. It is mainly visible in constant increasing of ICs integration scale, I/O (inputs/outputs) numbers, frequency and power density. Unfortunately, standard technologies of electronics interconnecting can not keep up with this trend and the technological gap appears (Figure 1.1), which puts into question the desirability of further miniaturization.

2. Packaging hierarchy and technologies

Microelectronics typically refers to those microdevices, such as integrated circuits, which are fabricated in sub-micron dimensions and which form the basis of all electronic products. “IC” is an abbreviation for “Integrated Circuit” and is defined as a miniature or microelectronic device that integrates such elements as transistors, resistors, and capacitors into an electrical circuit possessing a specific function. “Systems” refers to all electronic products. “Packaging” is defined as the bridge that interconnects the ICs and other components into a system-level board to form electronic products. This view of microelectronic systems is depicted in Figure 2.1. The overlap of ICs and Packaging is referred to as *Packaged Devices* or *IC Packaging* [1].

An example of “packaged device” technology is today's microprocessor in our PCs. The overlap of *Packaging* and *Systems* refers to incomplete or unintelligent system-level *Boards*, since these *Boards* do not contain the “brains” [the devices]. Finally, the overlap of *ICs* and *Systems* can be referred to as *Sub-Products.* These are considered as sub-products because they perform a partial function of th system, limited by the degree of integration at the IC level and yet they typically don't involve extensive packaging. These “sub” or complete products depend heavily on the level of integration of ICs independent of packaging in order to meet a variety of product functions. In the current evolution of systems technology, this approach evolved into a *system-on-chip* (SOC). A single chip radio is perhaps the best example of this. Most products, however, are based on a number of packaged ICs and other components assembled onto a system-level board. This is referred to as *system-on-board* (SOB). A new paradigm called *system-on-package* (SOP), or *system-in-package* (SIP) is analogous to SOC, in that it is a single component, multi-function, multi-chip package providing all the needed system-level functions. These functions include analog, digital, optical, RF and MEMS. Both SOC and SOP are expected to be the wave of the future.

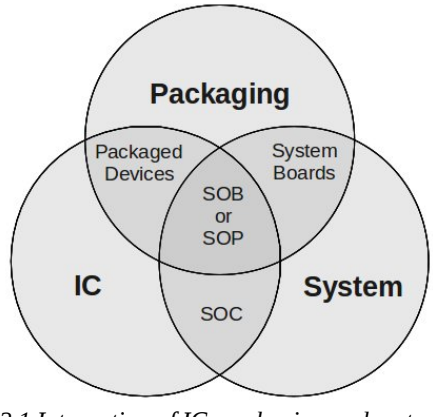


Figure 2.1 Integration of IC, packaging and system (After R. R. Tummala [1])

The most important advantages and properties of common substrate packaging (SOP or SOB) are:

- high design flexibility,
- possibility of applying heterogeneous technologies which properties are similar or even better than those used in SOC,

- ensuring of high yield, lower manufacturing costs and shorten *time-to-market*,
- high reliability caused by possibility of matching the coefficients of thermal expansion (CTE) of semiconductor chips and substrate,
- possibility of making the substrate embedded active and passive components,
- performance of connections between chips and substrate in the form of wire bonding or through silicon vias (TSV) provides fine pitch assembly.

Microsystems packaging involves two major functions: one at the IC or device level, and the other at the system-level. At the IC level, it involves interconnecting, powering, cooling and protecting ICs. At this level, typically referred to as *Level 1*, the packaging acts as an IC "carrier". The IC carrier, also called Packaged IC, allows ICs to be shipped "certified or qualified" by IC manufacturers after "burn-in" and electrical test to be "ready" for assembly onto a system-level board by end product or contract manufacturers.

Packaging a single IC does not generally lead to a complete system since a typical system requires a number of different active and passive devices. System-level packaging involves interconnection of all these components to be assembled on the system-level board, regardless of the type of component being assembled. The system-level board, also called "motherboard", not only carries these components on the top and below, but also interconnects every component with conductor wiring so as to form one interconnected system. This system-level board is typically referred to as *Level 2* in the *Packaging Hierarchy*.

In forming an electrically wired system-level board with assembled components, there are two additional interconnections that need to be made. First, the interconnection must occur at the *IC level* where the input/output (I/O) pads on the IC are connected to the first level of the packaging. This is typically done by wire bonding the components to a lead frame that has been fabricated to a specific shape in order to make it ready for interconnection to the next level of packaging. This is referred to as IC assembly. The second interconnection is typically achieved by means of solder bonding between the lead frame of the first-level package and electrically conductive pads on the second-level package, which is typically a "card" or "board". This is referred to as board assembly. The system-level board, with components assembled on either or both sides, typically completes the system.

There are products, such as mainframes and supercomputers, that require a very large number of ICs. By today's standards, a single system-level board may not carry all the components necessary to form that total system, since some of these require several processors to provide the extremely high transactional throughput. These types of systems might be used to manage large amounts of data such as an airline reservation system or a corporate mainframe network, or process high-resolution imagery such as with certain types of medical equipment. In this case, connectors and cables typically connect the several boards necessary to make the entire system. This is referred to as *Level 3* of Packaging [1]. The box, rack, or cabinet which houses the entire system is generally referred to as *Level 4* [4]. The *Three-Level Packaging Hierarchy* is illustrated in Figure 2.2. An example of level 4 of packaging is presented in Figure 2.3.

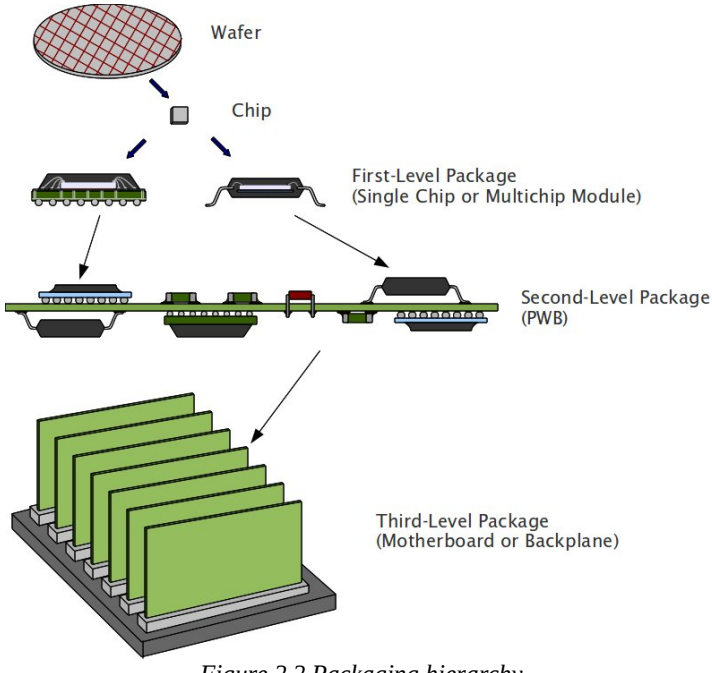


Figure 2.2 Packaging hierarchy

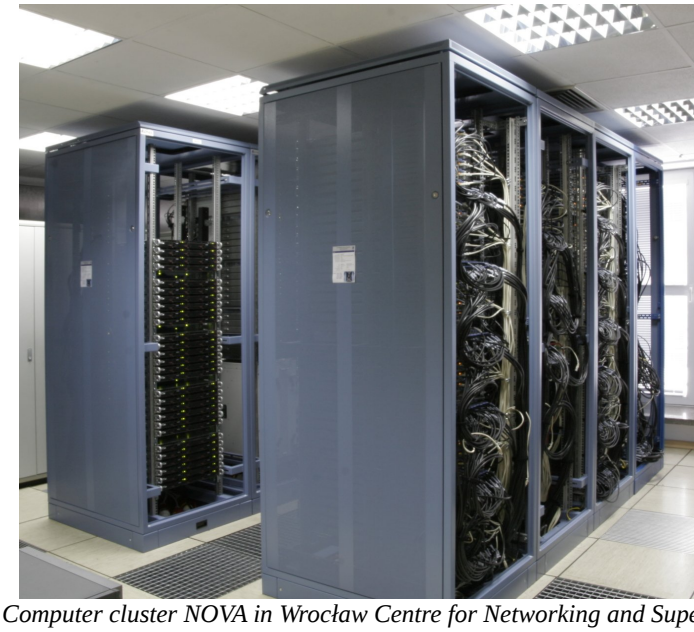


Figure 2.3 Computer cluster NOVA in Wrocław Centre for Networking and Supercomputing, (Courtesy of A. Kwiecień, WCSS)

Nowadays, small, light and reliable devices with an advanced functionality are in demand. One of the possibilities to achieve such features is the application of 3D stacked packaging. It is an electronic packaging in which the third (Z) dimension is used to stack the chips or packages on top of each other (Figure 2.4). In this way a surface on PCB can be saved and the functionality can be enhanced at the same time. Stacked packages may incorporate a standard flip-chip wafer that is bonded upside-down to a bottom silicon wafer prepared with through-silicon vias and/or standard wire bonding [5].

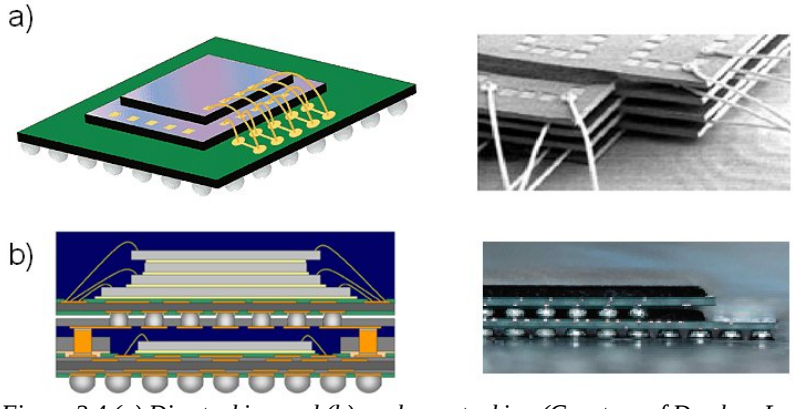


Figure 2.4 (a) Die stacking and (b) package stacking (Courtesy of Dowhan L. [5])

Today, the primary formats for stacked die packaging are 2-, 3-, and 4-wire bonded stacks, although stacks of 5, 6, and more are in development for low volume production. Stacked die are typically configured in a pyramid or same size stack, with overhanging designs. Currently, die as thin as 100 um are in production, with 50 um thick die in development. Typical stacked die packages contain 4 layers, with a BGA-type substrate and 70 µm to 80 µm pad pitch.

Two popular 3D chip scale package (CSP) device types are presented in Figure 2.5. In *PYRAMID* stack die configurations (Figure 2.5*a*), where a smaller die is placed on the top of a larger die, the wire loop from the top die needs sufficient clearance to the die edge of the bottom die as well as the lower loops. *Reverse bonding* can be used to solve this issue because reverse bonding offers sharp bend angle and higher bend height.

In the *SAME SIZE* stack die package (Figure 2.5*b*), where two or more dies of the same size are stacked with a spacer separating them, the edge of the top die is unsupported. Bonding to the overhang can cause die crack, loop damage and inconsistent bump formation due to die edge bouncing. Optimization of the wire bonding process can eliminate these problems. The most important wire bonding process parameters are constant velocity and bonding ultrasonic generator (USG) [6].

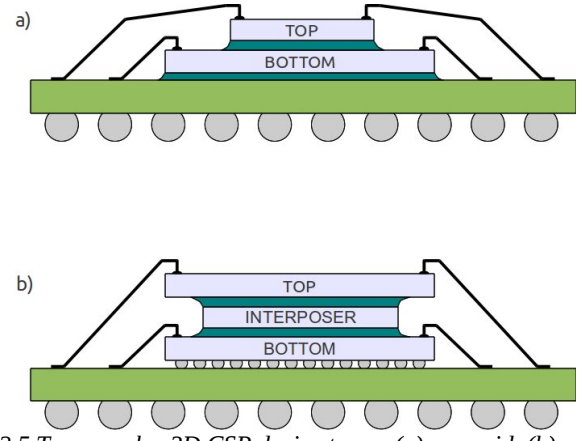


Figure 2.5 Two popular 3D CSP device types: (a) pyramid, (b) same size (After Kulicke & Soffa [6])

3. Wire bonding

Wire bonding is one of commonly used chip-to-package interconnection techniques. It is, by far, the most dominant form of electrical chip interconnection. Over $4 \cdot 10^{12}$ wire bonds are made annually. This staggering number of wire bonds accounts for well over 90 percent of all the first-level interconnections (chip to package or chip to board) produced [7].

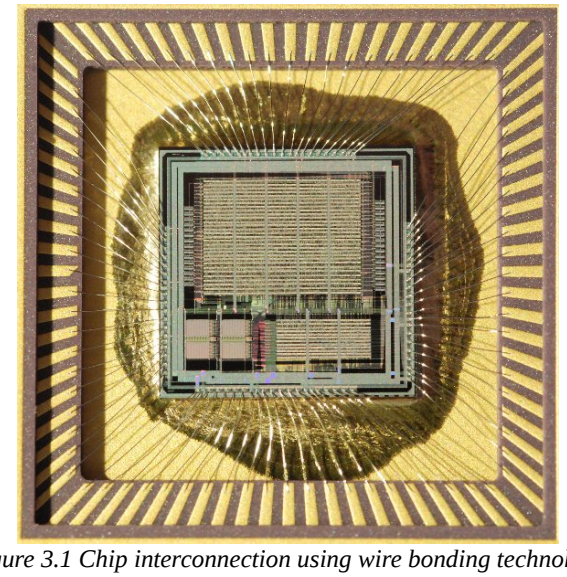


Figure 3.1 Chip interconnection using wire bonding technology (Courtesy of Stock.Xchng Photos)

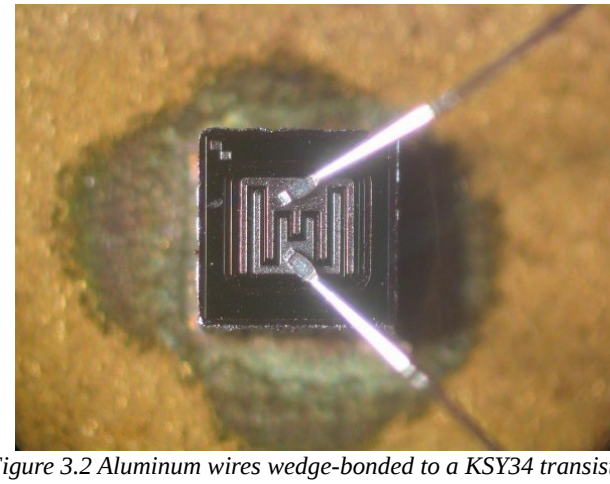


Figure 3.2 Aluminum wires wedge-bonded to a KSY34 transistor die (Courtesy of Wikimedia Commons)

For wire-bonded packages the chip interconnection process generally consists of two steps. In the first step, the back of the chip is mechanically attached to an appropriate mounting surface, for example, the lead frame in single-layer technologies (molded plastic and pressed ceramic) and the package chip cavity in the multilayer package technologies (laminated ceramic and plastic). This attachment sometimes enables electrical connections to be made to the backside of the chip. In the second step, the bond pads on the circuit side of the chip are electrically interconnected to the package by wire bonding. The wire bonding is performed with gold wire by thermosonic, thermocompression, or ultrasonic techniques, or with aluminum wire by the ultrasonic process [3].

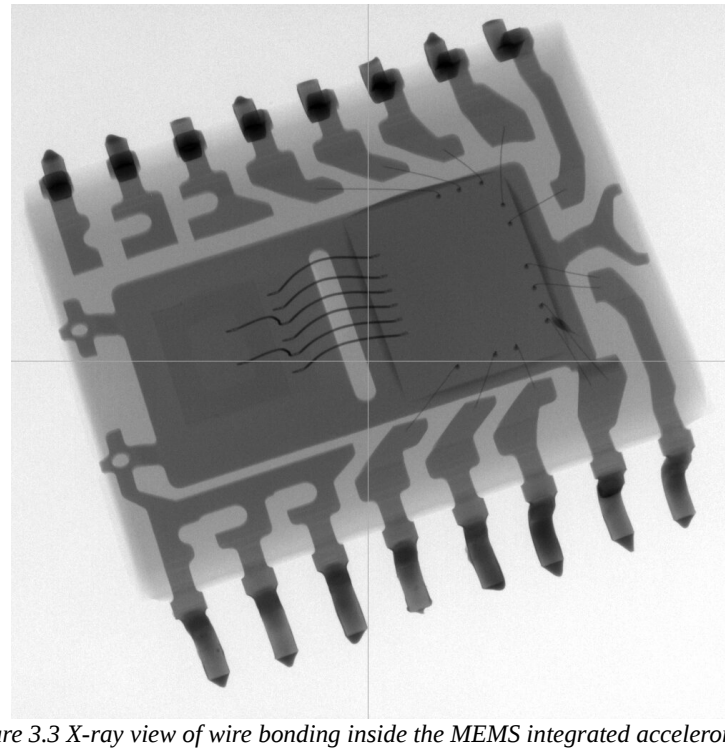


Figure 3.3 X-ray view of wire bonding inside the MEMS integrated accelerometer

A *thermocompression* bond (or weld) is the result of bringing two metal surfaces (bonding wire and the substrate or pad metalization, for example) together in intimate contact during a controlled time, temperature, and pressure (or force) cycle. During this “bonding” cycle, the wire and, to some extent, the underlying metalization undergo plastic deformation and interdiffusion on the atomic scale. This atomic interdiffusion can result in uniform gold welded interface, if both gold wire and gold pad or substrate metalization are used. Gold-aluminum intermetallics are formed when gold wire and aluminum pads (or vice versa) are used. Regardless, the plastic deformation that occurs at the bonding interface ensures: intimate surface contact between the wire and the pad, provides an increase in the interfacial bonding area, and breaks down any interfacial film layers (oxide, contamination, etc.). Surface roughness, voids, oxides, and absorbed chemical species or moisture layers can cause a poor bond. In some cases, this interfacial contamination is so extensive that it prevents bonding altogether [7].

The interfacial bonding temperatures are typically in the range of 300-400 ºC for bonds made by thermocompression bonding. The bonding cycle, exclusive of positioning, takes a fraction of a second. In thermocompression bonding, the required heat for interface formation is applied by either a heated capillary (the bonding tool through which the wire feeds) or by mounting the substrate and/or package on a heated stage (column) [7].

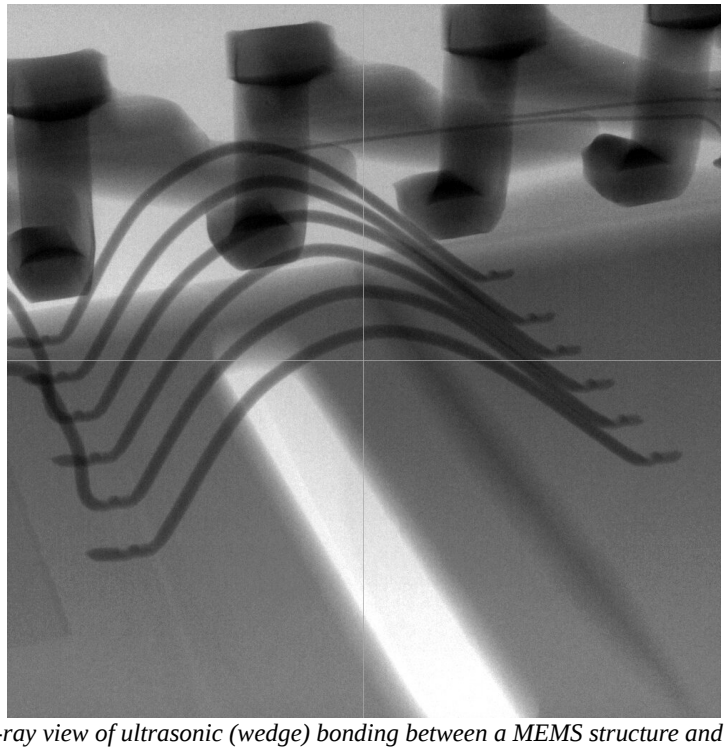


Figure 3.4 X-ray view of ultrasonic (wedge) bonding between a MEMS structure and a chip inside the integrated accelerometer

Ultrasonic bonding (or wedge bonding) is a lower-temperature process in which the source of energy for the metal welding is ultrasonic energy produced by a transducer vibrating the bonding tool (wedge) in the frequency range of 20 to 300 kHz. The most common frequency is 60 kHz, although higher frequency ultrasonics are in use or being considered for difficult bonding situations. In ultrasonic bonding, the wedge tip vibrates parallel to the bonding pad. Ultrasonic bonds are typically formed with aluminum or aluminum alloy wire on either aluminum or gold pads. Gold wire ultrasonic bonding has been performed with both round wire and flat ribbon, although it is not widely used because of cost. The major advantages of ultrasonic bonding include the ability to obtain strong bonds with little or no heat applied to the substrate (implying the use of low temperature die attachment methods); and it typically can be performed at finer pitches (because of the elongated, narrow shape of the bond compared to the round ball diameter) than ball bonding methods [7].

In *thermosonic wire bonding*, ultrasonic energy is combined with the ball bonding capillary technique employed in thermocompression bonding. Typically, the thermosonic bonding process is performed in a manner analogous to the thermocompression bonding process, except the capillary is

not heated (or held at a lower temperature when compared to the capillary temperature in thermocompression bonding); and the stage or column temperatures are typically 150 ºC or less. To generate the required interfacial heat for welding at the interface of the wire and the pad, short burst (tens of miliseconds) of ultrasonic energy are applied to the capillary when the wire and the pad are in contact. Because of the addition of ultrasonic energy (causing localized heat generation at the wire-pad interface), the requirements on the stage and capillary heat (as mentioned above) and pressure (force) can be relaxed. The applied forces in thermosonic bonding are typically much less than those encountered in thermocompression bonding, thus allowing bonding over a delicate or force sensitive chip or substrate regions. Since interconnections are made with the ICs (and substrates) held at temperatures of 150 ºC or less, they can be attached with epoxy or other organic adhesives without fear of degradation due to excessive bonder stage or column temperature. Because the temperatures are lower, there is also significantly less risk of uncontrolled intermetallic growth [7].

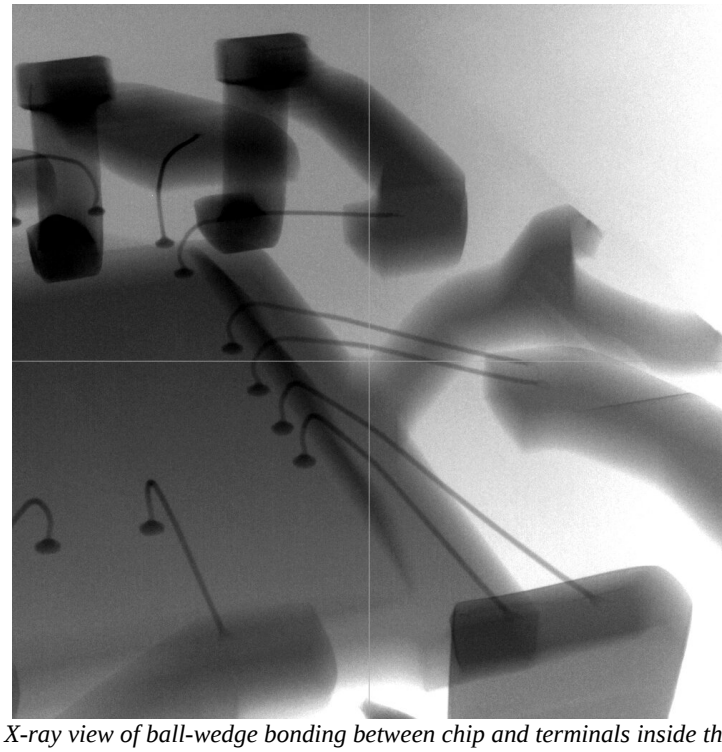


Figure 3.5 X-ray view of ball-wedge bonding between chip and terminals inside the integrated accelerometer

Typically, gold wire is ball-wedge bonded (thermocompression or thermosonic bonding), that is, ball-bonded to the chip bond pad (typically aluminum) and wedge-bonded to a plated lead frame or package (typically gold or silver plate), as shown in Figure 3.6. The wire bonding process begins with targeting the capillary on the bond pad and then positions above the die with a ball of which it is formed on the end of the wire (Figure 3.6*a*). The capillary descends, forcing the ball in contact with the die. An inside cone, or radius, grips the ball and forms the bond (Figure 3.6*b*). In a thermosonic system, ultrasound vibration is then applied. After the ball is bonded to the die, the

capillary raises to the position of loop height (Figure 3.6*c*). The clamps are open and the wire is free to feed out the end of the capillary. The lead of the device is positioned under the capillary, which is then lowered to the lead (Figure 3.6*d*). The wire is fed out the end of the capillary, forming a loop. The capillary deforms the wire against the lead producing a wedge-shaped bond, which has a gradual transition into the wire (Figure 3.6*e*). The capillary then raises away from the lead and leaves the stitch bond (Figure 3.6*f*). At a pre-set height the clamps are closed, while the capillary is still rising with the bonding lead. This prevents the wire from feeding out the capillary and pulls at the bond. The wire will break at bond's thinnest cross section. A new ball is formed on the tail of the wire, which extends from the end of the capillary (Figure 3.6*g*). A hydrogen flame or an electronic spark may be used to form the ball. The cycle is completed and ready for the next ball bond [3].

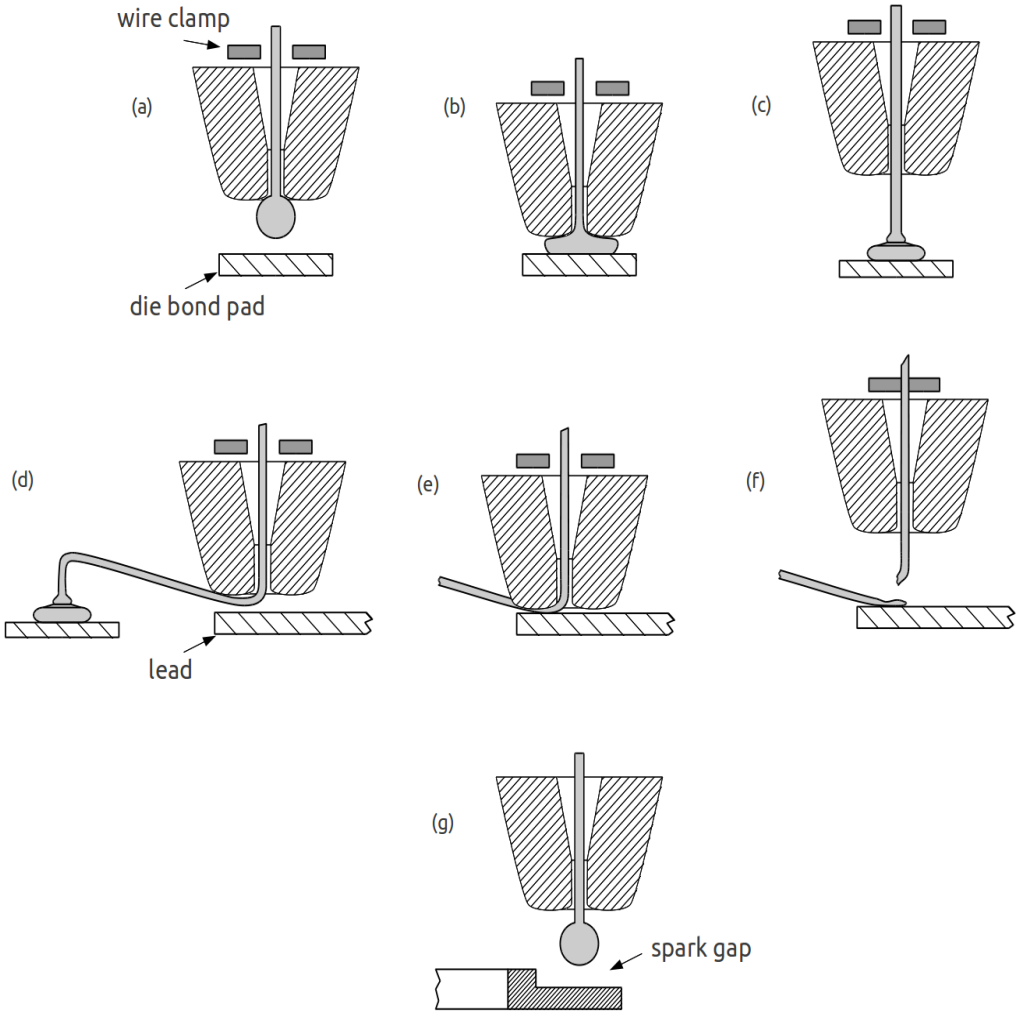


Figure 3.6 Tailless ball-and-wedge bonding cycle (After K. M. Striny [3])

One advantage of ball-wedge bonding comes from the symmetrical geometry of the capillary tip. The ball is formed by the inner portion of the tip (Figure 3.6*b*), and then the wedge bond can be formed anywhere on a 360° arc around the ball bond, using the outer portion of the tip (Figure 3.6*d* and *e*). This capability to draw the wire in any direction from the ball is the key factor that makes this process attractive for high-speed automated bonding, that is, the bonding head or package table does not have to rotate to form the wedge bond [3].

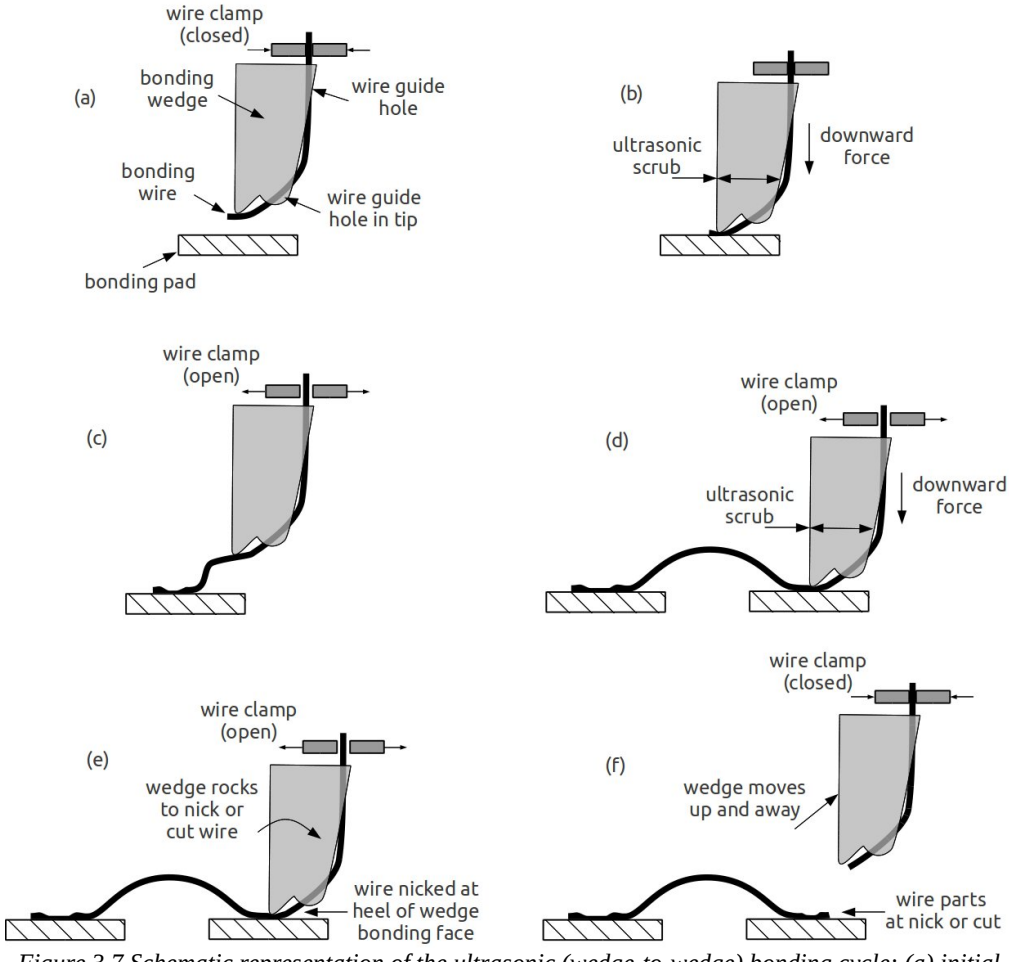


Figure 3.7 Schematic representation of the ultrasonic (wedge-to-wedge) bonding cycle: (a) initial wire-wedge configuration; (b) first bond; (c) transition to second bond; (d) second bond; (e) wire nicking or cutting operation; and (f) wire separation after second bond (After Charles H. K. [7])

Aluminum wire is typically wedge-to-wedge (ultrasonic) bonded. The ultrasonic wedge bonding process is illustrated in Figure 3.7.

The physical shape of a wedge bond suggests that a wedge-to-wedge configuration is limited to in-line bonding, that is, the orientation of the wedge bond at the chip determines the direction of the wire that terminates in the package wedge bond. This lack of versatility limits the automation

potential as mentioned. The complication of requiring motion in both the bonding head and the work holder results in a slower, more costly, and generally less reliable automatic bonding machine [3].

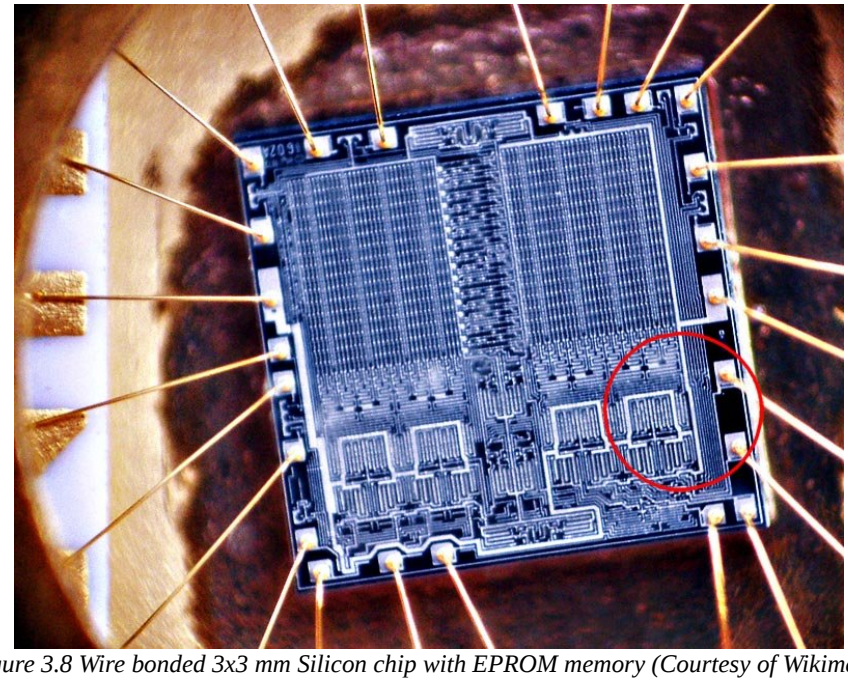


Figure 3.8 Wire bonded 3x3 mm Silicon chip with EPROM memory (Courtesy of Wikimedia Commons)

4. Flip Chip technology

One of the significant developments to improve cost, reliability and productivity in the electronic packaging industry has been the advancement of flip chip technology. The flip chip process was first introduced for ceramic substrates as the *Solid Logic Technology* by IBM in 1962. It was later, in 1970, that IBM converted this to the *Controlled Collapse Chip Connection*, or *C4*, for ICs. Flip chip technology is an advanced form of surface mount technology, in which bare semiconductor chips are turned upside down, and hence called *flip chip* (i.e. active face down), and bonded directly to a printed circuit board or to a chip carrier substrate. Development of solder-bump flip chip interconnections was initiated in an attempt to eliminate the expense, unreliability and low productivity of the manual wire bonding. In contrast to wire bonding, which is a peripheral and time consuming bond technique, in which bonds are formed sequentially, the flip chip allows all I/Os to be connected simultaneously.

Flip chip interconnection is the connection of an integrated circuit chip to a carrier or substrate with the active face of the chip facing toward the substrate. Interconnection between the chip I/O and substrate is achieved using a bump structure on the chip and a bonding material, typically on the substrate, forming an electrical interconnection between the chip and the substrate. Flip chip bonding typically involves solder interconnections that make the electrical and mechanical connection between the chip and the carrier, although alternate material systems such as conductive adhesives can also be used [8]. Schematic representation of a flip chip interconnection configuration is shown in Figure 4.1, where a bumped chip is interconnected to a substrate with the active face of the IC towards the substrate surface.

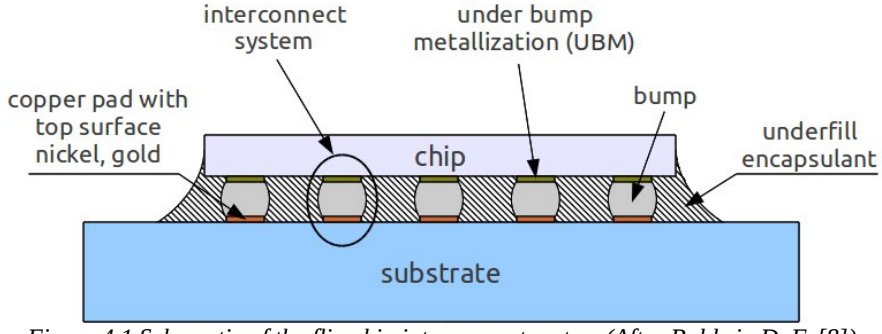


Figure 4.1 Schematic of the flip chip interconnect system (After Baldwin D. F. [8])

The substrate materials could be ceramic, epoxy-glass laminate, polymer thin-film build-up, *resin-coated copper* (RCC) build-up, glass, silicon, dielectric-coated metal, liquid crystal polymer, dielectric metal matrix composite, *low temperature co-fired ceramic* (LTCC), ceramic thick-film, multilayer high temperature co-fired ceramic, etc.

The flip chip packaging process generally includes wafer bumping and flip chip assembly. In the wafer bumping process, the peripheral pads on each chip in a wafer are redistributed to form area array pads. Under bump metallization (UBM) and solder bumps are then deposited on the redistributed pads. In the flip chip assembly process, bumped chips, after being diced from a wafer, are placed on a substrate and undergo a subsequent reflow process. Underfill is then deposited to reinforce the solder bumps and enhance the reliability of the flip chip package [9]. Schematic steps of flip chip interconnection process are presented in Figure 4.2.

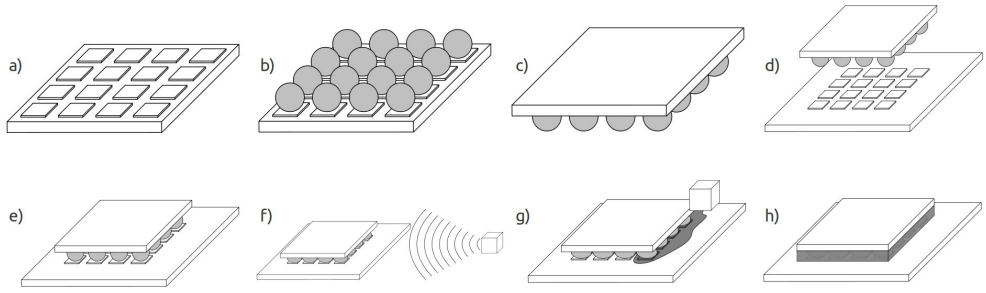


Figure 4.2 Process steps of flip chip interconnecting; (a) pad metalization on the chip surface; (b) deposition of solder dots on each of the pads; (c) chip flipping and (d, e) positioning so that the solder balls are facing the connectors on the substrate; (f) reflow process – remelting solder balls; (g, h) mounted chip is underfilled using electrically-insulating adhesive (Courtesy of Wikimedia Commons).

The under bump metallization (UBM) serves as a compatible layer between the bump metalization and final chip metallization. The most common final chip metallization is aluminum (Al), but gold is also used (mainly for GaAs applications), and copper (Cu) is gaining in popularity due to its improved electrical performance. The structure of the UBM (Figure 4.3) consists of an *adhesion layer* covering the chip metallization, a *barrier layer*, a *wetting layer*, and an *antioxidation barrier*.

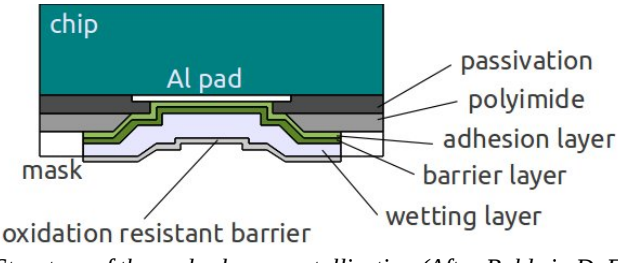


Figure 4.3 Structure of the under bump metallization (After Baldwin D. F. [8])

The under bump metallization is necessary for several reasons. A chip passivation is necessary to protect the Al metallized chip from moisture and corrosion. A polyimide layer is then applied for stress relaxation. The first metal layer is the *adhesion layer*. This metal must adhere to the aluminum oxide, the chip passivation, and the polyimide. It must also have low electrical contact resistance. Often, argon sputter etching of the Al surface is used to remove Al_2O_3 and reduces the interfacial resistance. In the original flip chip design, IBM recommended a 0.15 µm chromium layer. The second layer necessary is the *barrier layer*. This layer prevents the solder, primarily the tin, from migrating too quickly and corroding the aluminum device and/or dewetting the Cr layer during multiple reflows. Traditionally, a chrome/copper alloy has been used as a barrier layer (0.15 µm). The third layer deposited is the *wetting layer*. This layer, usually a thick layer of copper (1 µm), is necessary because the solder does not wet the metal deposited for the barrier layer nor the bare aluminum. Finally, a flash of gold is placed on the top of the wetting layer to inhibit

copper oxidation in a dual evaporation process. The UBM also helps prevent the corrosion of the chip metallization due to diffusion of contaminant ionics from the encapsulants and environment.

There are several processes for deposition of the UBM layers like evaporation and sputtering. Evaporation is a process based on the vaporization of a metal compound in a vacuum chamber, resulting in a uniform coating over the entire chamber surface, including the wafer. It requires pattering based on physical masks or lift-off techniques. Sputtering uses a directed metal ion plasma between an anode and cathode in a vacuum chamber, based on targets made from the materials to be deposited. Additional processes for deposition of UBMs are based on plating processes: *electrolytic plating* and *electroless plating*.

The UBM process is very costly and time consuming. In general, these metallization steps are completed in a clean, large area vacuum environment. In addition to the metal layers necessary for flip chip, an underfill, usually silica-filled epoxy, is typically applied between the joined chip and substrate. This underfill is completed after the solder is reflowed. Any rework and repair must be done before the application of the underfill. The underfill is needed to improve reliability. Because there is a mismatch in the coefficient of thermal expansion among the chip, the solder interconnections, and the substrate, stresses will be introduced. The underfill distributes the thermomechanical stresses over a larger area, significantly increasing reliability [8].

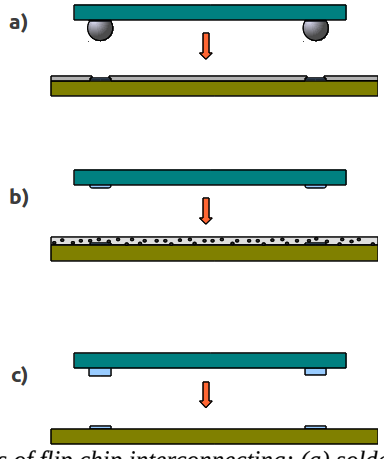


Figure 4.4 Methods of flip chip interconnecting: (a) soldering, (b) adhesive bonding, (c) thermocompression bonding

The bumps in a flip chip interconnection provide four functions: (1) electrical connection between the chip and substrate; (2) a heat dissipation path from the chip; (3) environmental protection; and (4) a structural line between the chip and the substrate. The materials and processes involved in the manufacture of the flip chip interconnection system determine its performance.

The most common materials used for bumping flip chip devices include solder, metallic stud bumps, and compliant polymer bumps. Schematics of the various types are shown in Figure 4.5. Solder bumps are deposited onto the UBM using several processes. The earliest process used was *evaporation*, developed by IBM for its flip chip technology. It requires a physical mask, typically molybdenum, that is aligned with the wafer I/O pads and released after deposition. The mask must have a draft angle though the apertures in order to remove the solder from the mask. A second process for deposition of solder is *electroplating*. The solder is electroplated through a polymer photoresist mask to control volume and registration. The bumps are reflowed after plating to homogenize the solder microstructure, since the electroplated solder is phase separated on

deposition. A third process for deposition of solder is based on *solder paste screening* or *printing*. Squeegee printing of specially designed solder paste can be accomplished using a precision stencil and automated stencil or screen printers. Bump printing can also be achieved using a polymer photoresist mask, however, the solder is doctor-bladed or squeeged into the holes in the resist. A third printing process commercialized is based on jet printing technology similar to ink jet printing used for document printing. In this case, molten solder drops are jetted onto the bond pads, forming the bumps. Solder jet printers can be configured for drop-on-demand deposition or the higher speed continuous drop deposition.

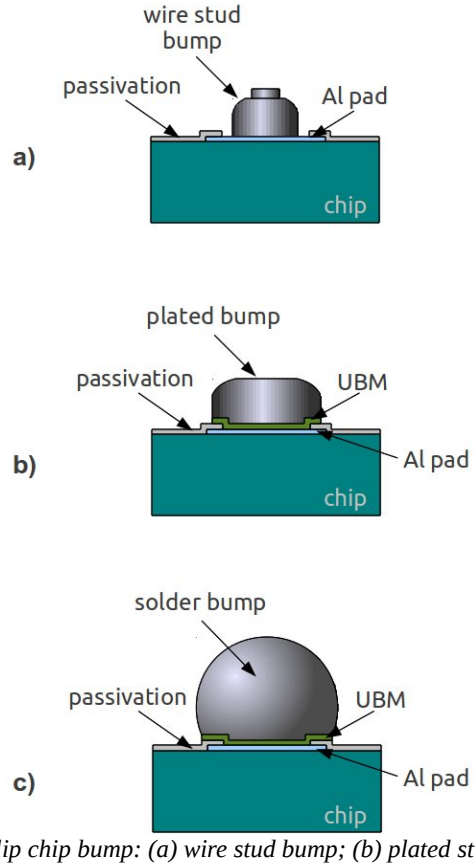


Figure 4.5 Flip chip bump: (a) wire stud bump; (b) plated stud bump; and (c) solder bump (After Baldwin D. F. [8])

Stud bumps can be plated or deposited using a wire stud bumping technique. Plated stud bumps are largely derived from the system used for tape-automated bonding (TAB) bumping, including gold, nickel, copper, gold-tin, nickel-gold, and nickel-copper. Both electrolytic and electroless plating techniques are used, where electroplating requires an electrical path for plating and achieves nearly an order of magnitude faster deposition rates. Wire stud bumps are formed using a ball bonding technique where the wire is fractured after ball bond formation. The wire stud bumps can be coined to form a uniform structure for bonding. The most common wire stud bumps

are made with 25 µm diameter gold wire. An example of a wire stud bumps is shown in Figure 4.6.

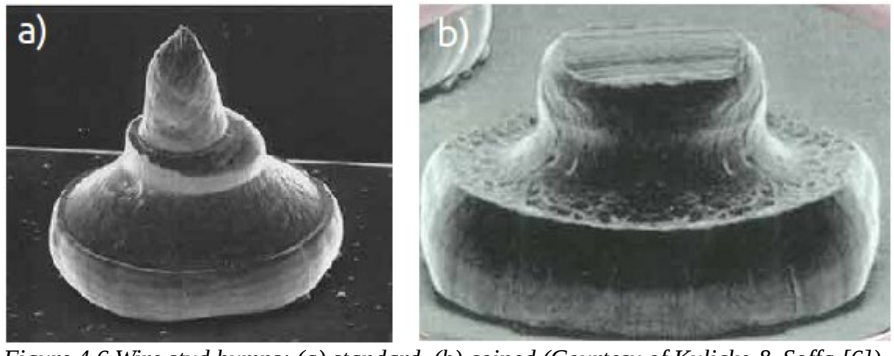


Figure 4.6 Wire stud bumps; (a) standard, (b) coined (Courtesy of Kulicke & Soffa [6])

5. Printed circuit boards

5.1. System-level printed circuit board

A printed circuit board (PCB) or printed wiring board (PWB) is a composite of organic and inorganic materials with external and internal wiring, allowing electronic components to be electrically interconnected and mechanically supported. In addition, a PWB must provide power to the components and conduct away the heat when necessary. The boards are also called motherboards or system-level boards, because they carry all of the components required for that system or subsystem. They are also called back planes when some of the boards are interconnected to a larger motherboard. The terms “printed circuit board” and “printed wiring board” are synonymous [10].

The earliest “printed circuits” were made by printing a pattern of rubber-like resist on a copper plane, followed by etching. A laminate material made of phenolic and paper supported the copper. Holes punched in the laminate held the component leads which were soldered to the copper-printed pattern. Therefore, the printed circuits provided mechanical support and electrical interconnection for the components. The earliest developments of this nature were credited to Paul Eisler in the early 1940s when he was able to image copper circuity using gelatin and ferric chloride etchant [10].

5.2. Types of printed wiring boards

Printed circuit boards are typically less than 0.1 mm to several millimeters thick. The thinner laminates are used for pagers, mobile phones and calculators, whereas those in the mid-range of 0.5 mm, are found in notebook computers, camcorders and radios. Thicker PCBs are used in printers, TVs, and are prevalent in personal computers and workstations. The thickest multilayers are found in office computers, mainframes, and telecommunications switches. Their thickness typically relates to the number of laminated layers, which is determined by both the number of components and their I/O (Input/Output) to be interconnected. For example, a mainframe of past era used 47 layers of PCB, because it had to interconnect over 300 VLSI (Very Large Scale Integrated) packages, each with more than 500 I/Os [10]. VLSI BGA packages are presented in Figure 5.1 [11].

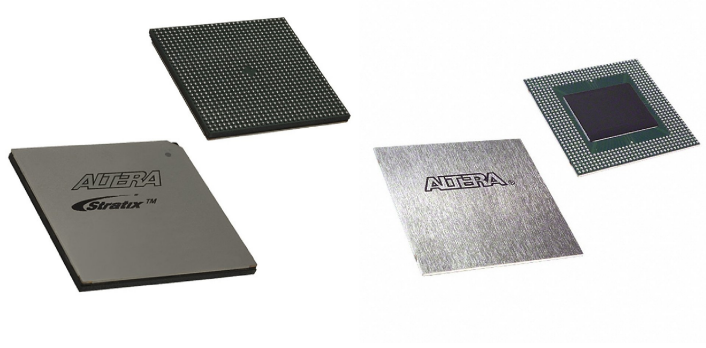


Figure 5.1 VLSI BGA packages (Courtesy Digi-Key Corporation [11])

Chip carriers are single-chip packages that include wirebond, tape automated bonding (TAB), and flip-chip bonded IC packages. They are both polymer-based and ceramic-based materials. The polymer-based ones are largely epoxy-glass based because of their low cost [10].

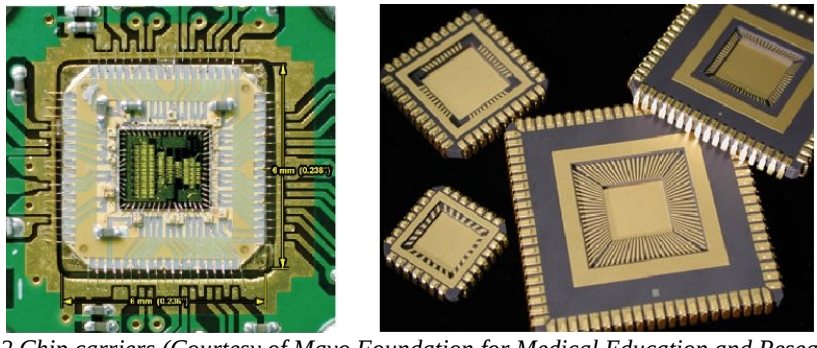


Figure 5.2 Chip carriers (Courtesy of Mayo Foundation for Medical Education and Research [12])

Flexible-circuits are printed circuits deposited on a flexible dry film. These films are predominantly made of polyimide and polyester-based materials. Their adaptability to roll handling manufacturing, and high-density conductor capability by photolitography, makes them popular for 3-D consumer applications such as cameras, disk drives and older telephones [10].

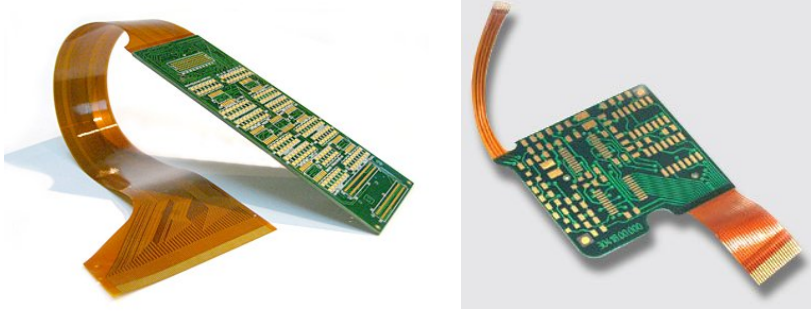


Figure 5.3 Flexible circuits (Courtesy of All Products Online Corp. [13])

Metal core boards are the boards with metal as the base material, on which glass or polymer is deposited as the insulator and conductive paste, or thin-film metal is deposited to serve as the conductor. The metal boards are used in special applications where either high temperature, as in automotive, or high heat dissipation, as in power supplies, is required [10].

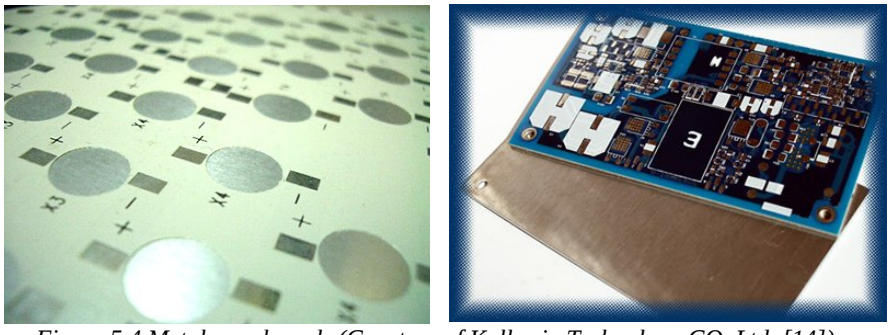


Figure 5.4 Metal core boards (Courtesy of Kollewin Technology CO. Ltd. [14])

5.3. Categorizing of printed circuit boards

The main criteria for selecting and categorizing printed circuit boards are as follows [10]:

- rigidity of the insulating board: rigid, flexible or combined (rigid-flex),
- number of conductive layers: single-sided, double-sided or multilayer, such PCBs are presented in the Fig 5.5, 5.6 and 5.7

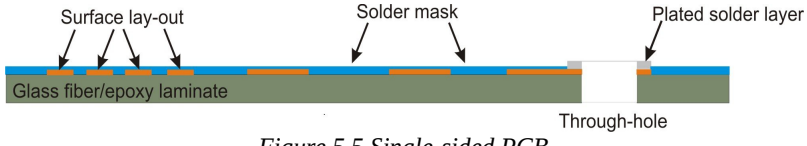


Figure 5.5 Single-sided PCB

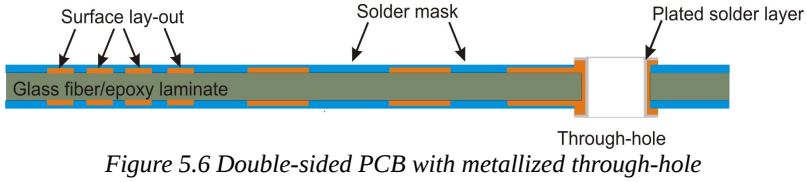


Figure 5.6 Double-sided PCB with metallized through-hole

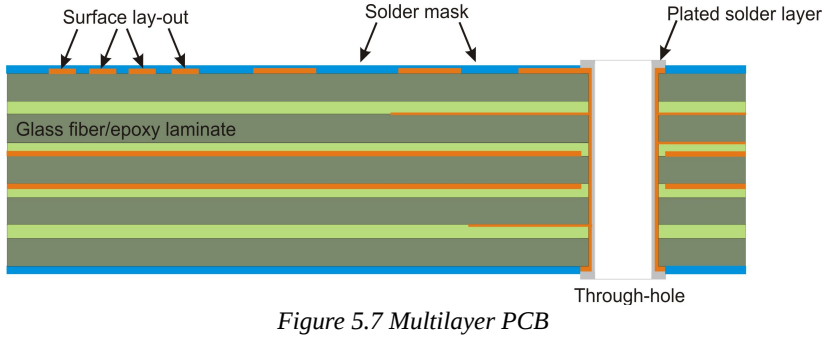


Figure 5.7 Multilayer PCB

- role and type of holes: non-metallized, plated through holes (PTHs) or vias (including through board), blind and buried vias such as, the PCBs presented in the figures below.

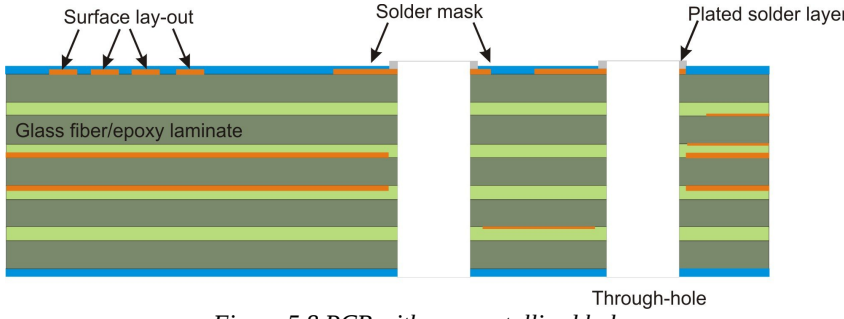


Figure 5.8 PCB with non-metallized holes

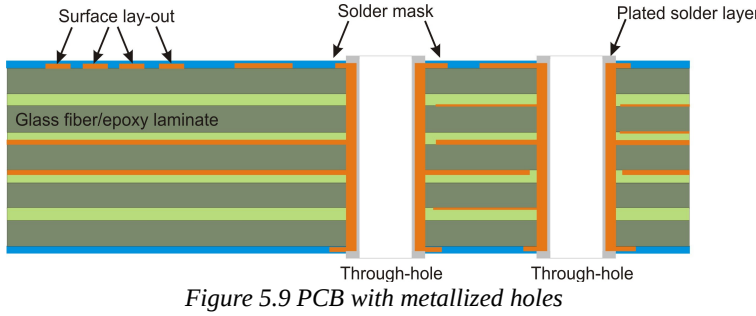


Figure 5.9 PCB with metallized holes

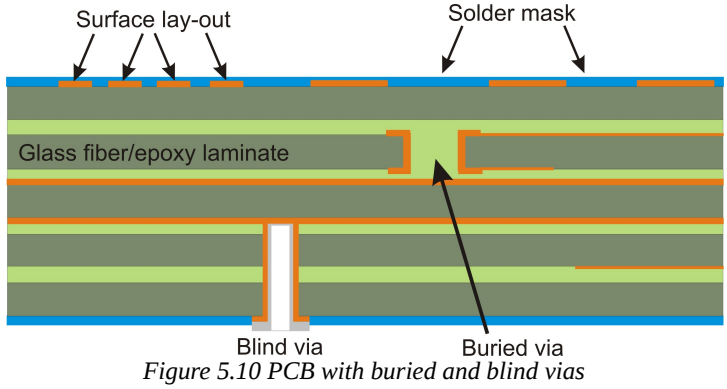


Figure 5.10 PCB with buried and blind vias

A multilayer structure with different vias is presented in Figure 5.11.

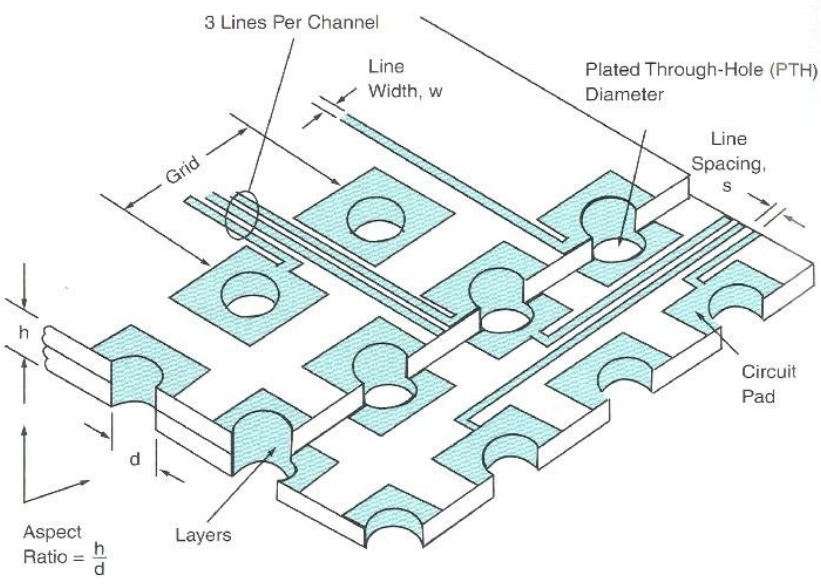


Figure 5.11 PCB with different vias and marked parameters [1]

Wiring capability of printed circuit board can be calculated as:

$$Wiring\ capability = \frac{(Lines\ per\ channel)(Layers)}{Grid}.$$

Wireability is a measure of package capability to provide interconnections between components. The total wireability of a package can be calculated as:

$$Wiring = (Number\ of\ lines/channel)\,x\,(number\ of\ channels/cm)\,x\,(Number\ of\ signal\ planes).$$

- quality of the conductive pattern: coarse, fine or very fine,
- type of connector: edge connector, other standards.

The evolution of high-density interconnect is presented in Table 5.1.

Table 5.1 Types of structures and the evolution of high-density interconnect [15]

Horizontal Placement		Wire Bonding Type; Flip Chip Type
Stacked Structure	Interposer Type	Wire Bonding Type; Wire Bonding + Flip Chip Type; Flip Chip Type
	Interposer-less Type	Terminal Through Via Type
Embedded Structure		Chip Embedded + Chip on Surface Type; 3D Chip Embedded Type

5.4. Materials of standard printed circuit boards

The three key components of standard printed circuit boards are [10]:

- organic resin,
- inorganic filler,
- copper conductor.

The laminate material, which is used in printed circuit board manufacturing, is a sandwich structure of conductors and dielectrics. The wiring pattern is produced in the conducting plane by etching-in high electrical conductivity patches, whereas the dielectric supporting the patches should be a good insulator [10]. Elements of a PCB substrate is presented in Figure 5.12.

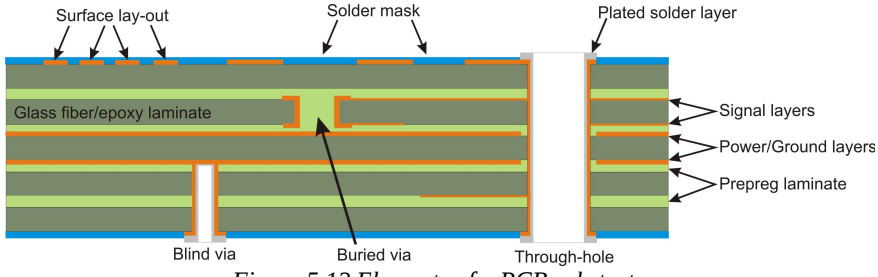


Figure 5.12 Elements of a PCB substrate

Moreover, depending on the destination, a substrate material of PCB should fulfill the following requirements [16]:

- ensure compatibility of coefficients of thermal expansion of substrates and components,
- high thermal conductivity,
- ensure dense interconnections,
- low dielectric constant.

The conductor should be fabricated of materials with extremely high electrical conductivity and should be solderable, etchable and manufacturable in small lines and spaces. The most common is copper [10].

The insulator selected should [10]:

- have high insulation resistance and breakdown voltage,
- have good mechanical strength,
- withstand corrosive chemicals used in processing,
- not absorb water,
- not degrade at process temperatures,
- be able to drill through,
- not expand too much in the Z-direction,
- be able to dissipate heat in product use.

The base material, or the insulating board of a rigid printed wiring board, is a sheet of laminate reinforced resin. A large majority of the laminates are produced using epoxy, but less frequently phenolic, and polyimide resins are also in use for advanced applications. The reinforcing materials, or the fillers, are typically glass cloth, paper, aramid, nylon and so on. Table 5.2 provides information about the main parameters including the glass transition temperature (Tg), which is defined as the temperature at which an amorphous polymer changes from a hard and relatively brittle condition to a viscous or rubbery condition. When this transition occurs, many physical

properties such as hardness, brittleness, elastic modulus, coefficient of thermal expansion (CTE), and specific heat undergo significant changes [10]. The anatomy of FR-4 printed circuit board is presented in Figure 5.13.

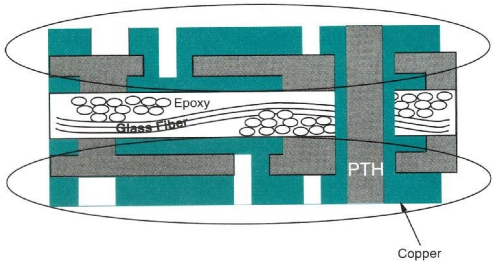


Figure 5.13 Anatomy of FR-4 PCB [1]

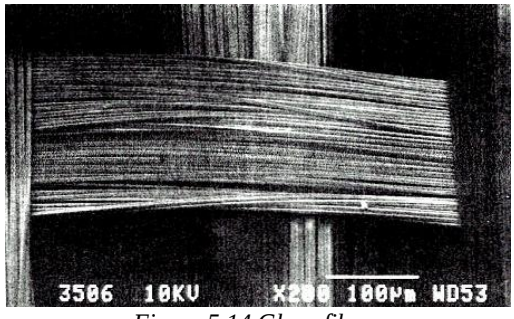


Figure 5.14 Glass-fibers

The FR-4 epoxy-fiberglass laminate (FR-4 is a widely accepted international grade designation for fiberglass reinforced epoxy laminates that are Flame Retardant) is the standard printed wiring board material for most board applications because of its acceptable dimensional stability, heat resistance, good adhesion and large area processability, resulting in low cost. Temperature of glass transition is 120-135°C, which is acceptable in most of applications. The value of coefficient of thermal expansion is similar to copper – about 16 ppm/K.

Polyimide-epoxy-resins are also used with fiberglass reinforcement for some special rigid PCBs requiring higher temperature for assembly, as they retain flexural strength up to 350°C or higher. The polyimide laminates are more expensive than their epoxy equivalents [10].

Resin systems provide the bond between the copper and the filler, and have a strong influence on the final electrical, mechanical and physical properties of the multilayer structure. Typical resin system properties (glass transition temperature *Tg* and lateral coefficient of thermal expansion *CTE*) are shown in table 5.2 [10]. Resin systems are moving toward higher glass transition temperature and better electrical properties than conventional epoxy. The reliability of the high temperature glass transition epoxy boards is improved over the standard ones.

Table 5.2: Typical resin system properties [10]

Resin / Filler	Tg (°C)	Lateral CTE (ppm/K)
Phenolic / Paper	135	14...18
Epoxy / Glass (FR-4)	130	14...18
Polyimide / Glass	250	12...16
Polyimide / Quartz	280	6...8
Epoxy / Aramid	180	7...9
BT-Epoxy	185	13...14
Cyanate Ester	240	-
Polyimide / Aramid	230	7...9

The filler material provides the mechanical rigidity of laminates. Composition of three typical glass fibers are shown in table 5.3 [10].

Table 5.3: Composition of three typical glass fiber (in wt%) [10]

	E-glass	S-glass	D-glass
SiO_2	52 – 56	64 – 66	73 – 75
$Al2O_3$	12 – 16	22 – 24	0 – 1
CaO	15 – 25	<0.01	0 – 2
MgO	0 – 6	10 – 12	0 – 2
B_2O_3	8 – 13	<0.01	18 – 21
Fe_2O_3	-	0,1	
Zr_2O_3	-	<0.1	

5.5. Manufacture of printed circuit boards

The boards produced with one or both sides covered by copper foil are called copper clad laminates. The thickness of the copper foil most commonly used is 35 μm, but for fine line circuits foils as thin as 5 μm are also in use. The adhesion of the foil to the organic reinforced prepreg (pre-impregnated laminates) is achieved during the lamination process. The granular side of the foil is pressed to the resin of the laminate and cured at increased temperature [10].
The major raw materials required for producing a standard FR-4 grade laminate are [10]:

- epoxy-resin suitably blended,
- filler material in the form of glass cloth,
- copper foil of required thickness.

The first stage of laminate production is compounding. The epoxy-resin is activated by mixing together precise amounts of the resin components. In order to increase mechanical rigidity of the final laminate, the resin is reinforced with glass fabric as filler material. The fiberglass cloth is impregnated with semi-cured epoxy-resin. Semi-cured prepregs are cut to 4-up size and covered with copper foil. The final stage operation is the final curing after laminating the copper foil to the prepreg material. The production process of laminates is presented in Figure 5.15 [10].

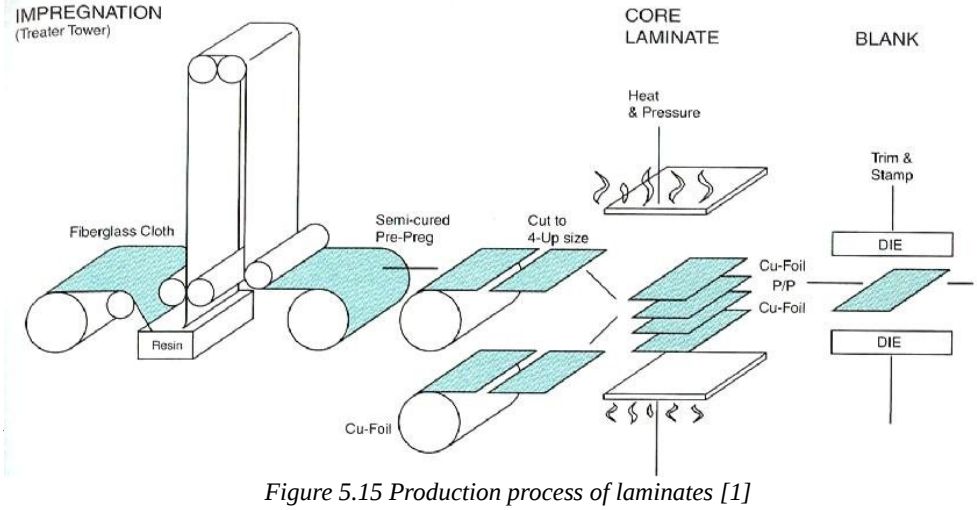


Figure 5.15 Production process of laminates [1]

A standard printed circuit board process sequence is as follows [10]:

- CAD output technology files,
- prepare mask,
- fabrication of interconnect pattern on the surface of PCB:
  - prepare copper clad laminate (cleaning, brushing),
  - apply photoresist on laminate,
  - image (exposure, develop) using the mask,
  - strip resist,
  - sub-etch pattern,
- repeat previous steps if necessary (multilayer PCBs),
- drill holes,
- through-hole plate for double sided and multilayer boards,
- protect copper with coating (ENIG – electroless nickel immersion gold, HASL – hot air soldering level, OSP – organic solderability preservative , ImSn – immersion tin, ImAg – immersion silver, etc.),
- solder mask/legend print.

When pattern transfer image is plated the method is additive, otherwise, when pattern image is etched the method is subtractive. The photoresist materials are either liquids or dry films of an initial system.

The purpose of drilling is to produce an opening through the board which will permit a subsequent process to form an electrical connection between the top, bottom, and, sometimes intermediate conductor pathways, and to permit through-hole component mounting. The elements of the laminate drilling process are drill entry and backup foils, drill bits and equipment-related parameters. Drill bits are usually made of tungsten carbide. Representative operating ranges in the industry are spindle speeds of 50000-100000 rpm, a feed of from 50-400 cm/min, and high reaction rate [10].

A major part of manufacturing involves the wet process. The plating aspects of wet chemistry include deposition of metals in electroless and electrolytic processes. The steps involved in the electroless copper plating include cleaning, copper microetching, hole and surface catalization with palladium, and electroless copper plating by using a reducing agent like formaldehyde. Electroplating is also used to protect copper by plating Sn, and by deposition of nickel as a solder barrier undercoat, prior to the application of gold in selected areas of the board [10].

The most common chemical etching systems are based on alkaline ammonia, hydrogen peroxide-sulfuric acid, and cupric chloride. Other systems include persulfates, ferric chloride and chromic-sulfuric acids. The process steps include [10]:

- resist stripping,
- precleaning,
- etching,
- neutralization,
- water rinsing,
- drying.

In order to produce multilayer PCBs many additional technological operations must be done which enable accomplishment electrical connections between the layers. First, the panels with the inner conductive layers are produced by simple double-sided etching from copper clad prepreg laminates. Then, these etched panels, adhesive prepregs and unetched outer panels are laminated,

pressed and cured (heat treated) to get a rigid board. Finally, this board is processed by a sequence of process steps corresponding to the pattern or panel plating of double-sided boards [10].

There are three primary types of solder resist masks in use today. They are:

- screen-printed,
- dry film,
- liquid photoimageable (LPI).

All exposed copper surfaces not covered by solder mask need to be protected by one of the finishes [10]:

- electroplated nickel + matte tin, its benefit is solderable surface and good shelf life,
- electroplated nickel + hard gold, its benefit is excellent corrosion resistance, shelf life, hardness and wear resistance,
- electroplated nickel + soft gold, its benefit is excellent corrosion resistance, shelf life, fair wear resistance, good for pressure contacts and aluminum or gold wirebonding,
- electroless plated nickel + immersion gold, its benefit is excellent corrosion resistance, solderability shelf life, good for aluminum wirebonding and for fine-pitch technology,
- hot air solder leveling (HASL), its benefit is excellent solderability, good shelf life,
- organic solderability preservatives (OSP), its benefits is solderability, surface coplanarity and hole size uniformity, good shelf life, excellent for use in fine-pitch technology.

A process flow of PCBs fabrication is presented in Figure 5.16.

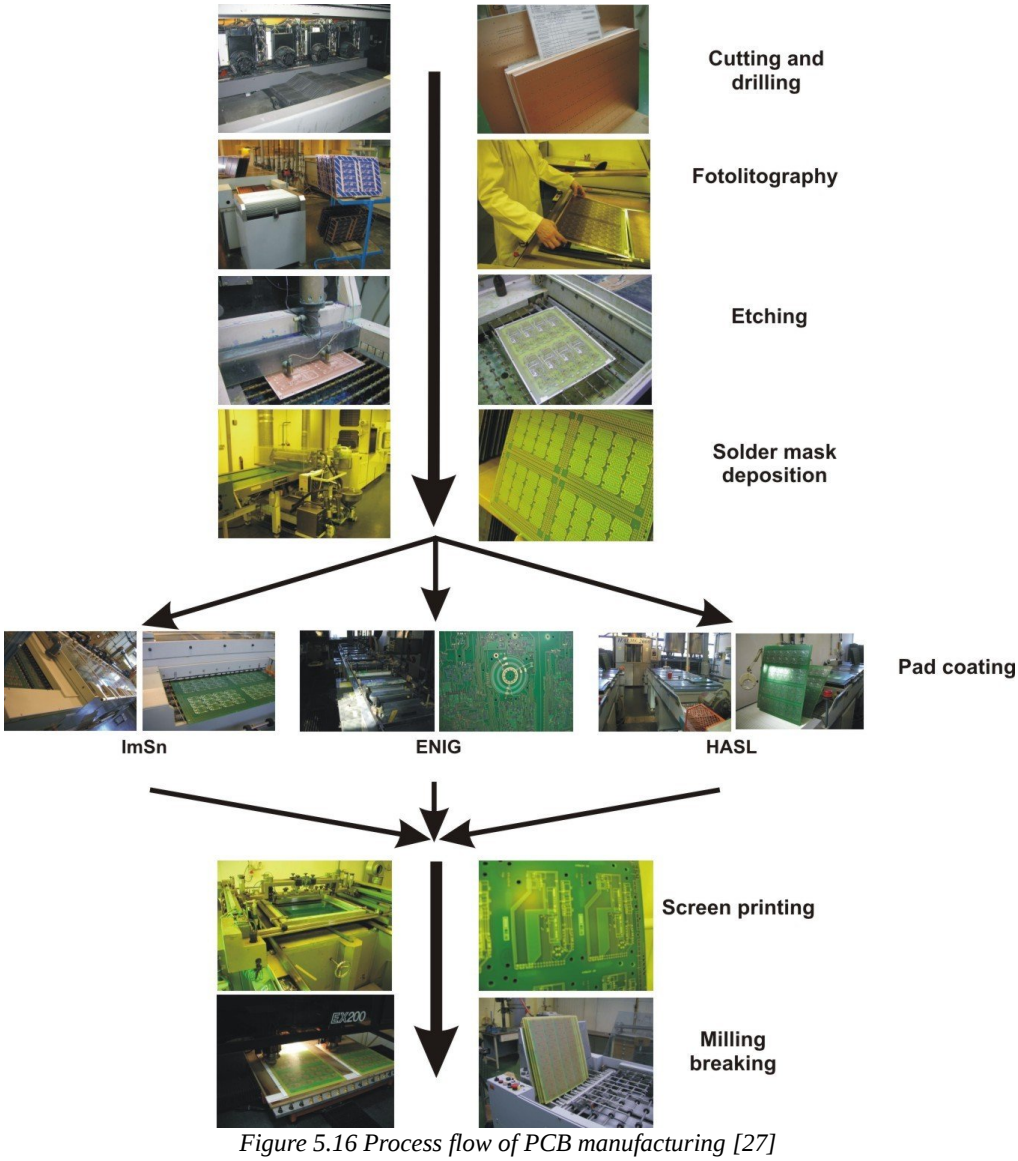


Figure 5.16 Process flow of PCB manufacturing [27]

6. Passive and active components for packaging

IC package designs have proliferated over the years into a wide variety of shapes, sizes, number of I/O pins, lead arrangements, and geometries in response to circuit- and system-level demands. This proliferation of package types becomes very uneconomical to end users; for example, original equipment manufacturers (OEMs) using electrically equivalent components from different suppliers must use several PCB designs because the components are in different packages. Assembled packages need to be handled economically and with special precautions, such as electrostatic protection, through a series of back-end processes that include lead trim and form, code marking, electrical testing, electrical burn-in, shipping, and subsequent assembly to the next level of packaging. This activities need major industry support in the development of specialized custom equipment and tooling, for example, magazines, sticks, trays, or tape for handling through the back end, test sockets for production start-up testing, test sockets and boards for device burn-in, test handlers and electrical contacts for production testing, and automatic placement and insertion equipment for component board assembly. The industry has been very active in the standardization of IC package outlines, which resulted in footprint and handling compatibility of components from different vendors and the focusing of the support activities on fewer package types, hence optimizing the overall economics of electronics packaging [3].

According to the classification of electronic packaging hierarchy, the second level relates the assembly of bare die or molded structures of ICs, discrete components and microsystems to printed circuit boards (PCBs). In the series production the assembly of bare die structures are avoided and more and more attention is paid for efficient and highly precise automatic assembly. It requires unified packages and component sizes.

The packages of electronic components (both discrete as well as ICs) can be classified according to the technology used to assembly on PCB, i.e. *through-hole technology* (THT), and *surface-mount technology* (SMT). It is noteworthy that this distinction covers discrete components as well as ICs. These two categories refer to the methodology used in assembling the packages to the PCB. If the packages have pins that can be inserted into holes in the PCB, they are call*ed through-hole* packages. If the packages are not inserted into PCB, but are mounted on the surface of the PCB, they are called *surface mount* packages. The advantage of the surface mount package, as compared to through-hole, is that both sides of the PCB can be used, and therefore, higher packaging density can be achieved on the board [2].

6.1. Through-hole technology

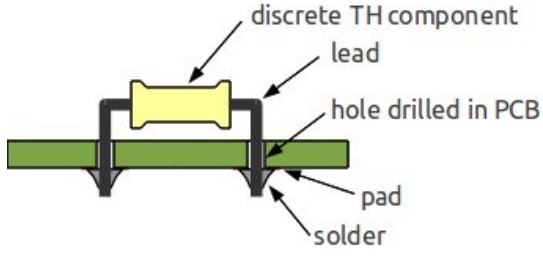


Figure 6.1 Schematic of through-hole mounted discrete component

In through-hole technology electronic components are assembled into an electronic circuit by inserting their leads into pre-drilled holes on the PCBs on one side, and soldered to the pads on the opposite side (Figure 6.1). The circuits can be assembled manually by hand placement or by the use of automated insertion mount.

6.1.1. Discrete devices

Discrete devices (i.e. electronic components with just one passive or active circuit element) are produced as either axial-leaded (Figure 6.2), radial-leaded (Figure 6.3) or multi-leaded (Figure 6.4) parts. The axial-leaded through-hole parts are mounted horizontally by bending the leads 90 degrees in the same direction before inserting them into the holes in PCB. The radial-leaded parts have the leads already formed in the same direction, so they do not require bending leads step before assembly.

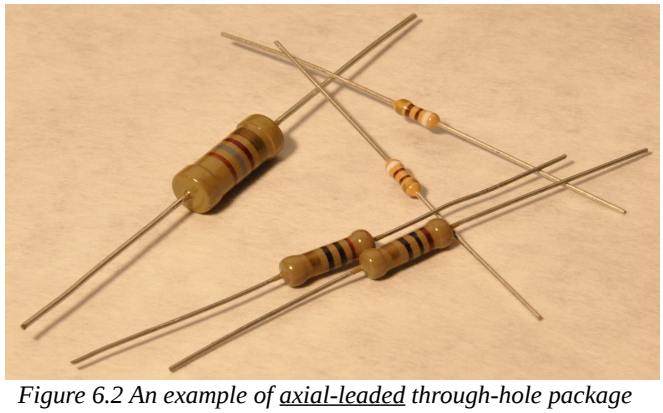


Figure 6.2 An example of axial-leaded through-hole package

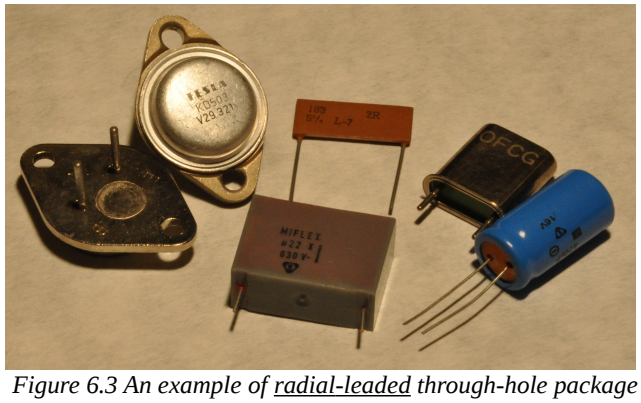


Figure 6.3 An example of radial-leaded through-hole package

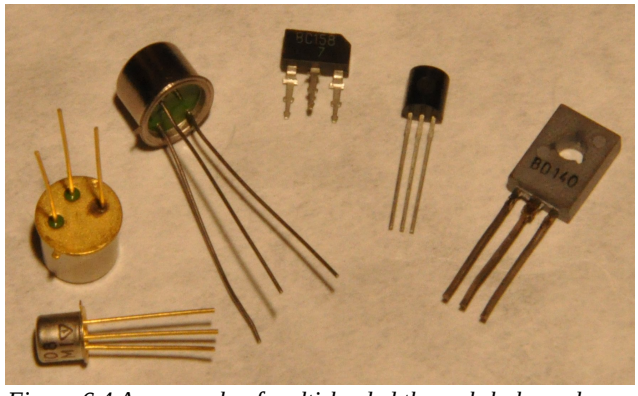


Figure 6.4 An example of multi-leaded through-hole package

6.1.2. Integrated circuits

Since there are many types of ICs and IC requirements it is impractical to have one package solution for all ICs. To resolve this problem, many types of IC package technologies have been developed that vary in their structures, materials, fabrication methodology, bonding technologies, size, thickness, number of I/O connections, heat removal capability, electrical performance, reliability, and cost [2].

It is worth to notice that there is a distinction between a single chip and multichip packaging. A *single chip package* (SCP) is a package that supports a single microelectronic device so that its electrical, mechanical, thermal, and chemical performance needs are adequately served. The device so packaged as illustrated in Figure 6.5 originates from a wafer, gently singulated or diced, then packaged, burnt-in and tested. Such a packaged IC may contain millions of transistors. An easily recognizable example of a SCP is Intel's *ceramic pin grid array* (CPGA) that has been used to package multiple generations of the X86 family of microprocessors (Figure 6.6) for personal computers. If the package contains more than one active device, it is called a *multichip package* (MCP) or *multichip module* (MCM). The system designers may utilize a combination of passive components, SCPs, and MCMs to meet the specific application needs of the system [17].

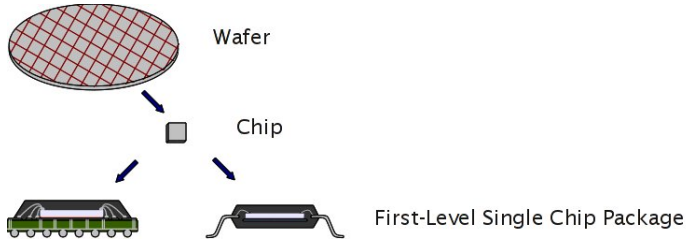


Figure 6.5 Single Chip package process from wafer to shippable IC

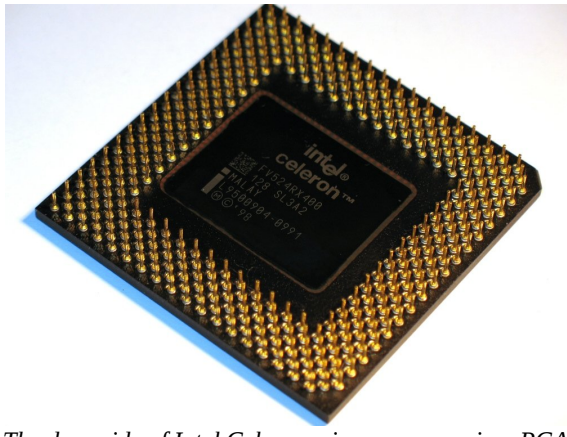


Figure 6.6 The downside of Intel Celeron microprocessor in a PGA packaging (Courtesy of Wikimedia Commons)

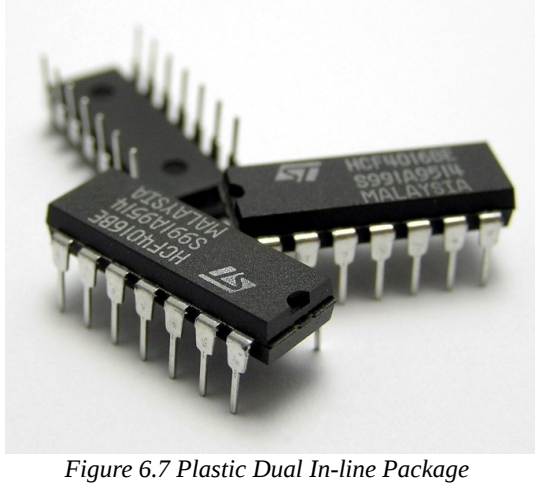


Figure 6.7 Plastic Dual In-line Package (Courtesy of Wikimedia Commons)

The most common through-hole packages of ICs are *Dual In-line Package* (DIP; sometimes called a DIL-package for Dual In-Line package) and *Pin Grid Arrays* (PGA). The DIP (Figures 6.7 and 6.8) was the first package invented by Bryant Rogers of Fairchild in the early 1960s with 14 leads and was quickly adopted by Texas Instruments in 1962. The DIP comes in either plastic or ceramic version, and was one of the earliest industry standard, commodity packages for low pin counts, usually in the 8 to 48 pin range. The applications include memory and logic microcontrollers. The package is fully encapsulated in a molding compound, and the interconnect to the next level is provided by copper or Kovar™ leadframe, with lead pitches of 1.75 and 2.5 mm. DIP is not preferred when space is a critical design constraint [17].

Figure 6.8 Ceramic Dual In-line Package

In DIPs, the I/Os, or the pins, are distributed along the sides of the package. To achieve higher I/O connections, PGAs (Figure 6.6) are used where the pins are distributed in an area array fashion underneath the package surface [2]. The pins are commonly spaced 2.54 mm (0.1") apart, and may or may not cover the entire underside of the package. PGAs are often mounted on printed circuit boards using the through hole method or inserted into a socket.

The whole family of through-hole ceramic as well as plastic packages is presented in Figures 6.9 and 6.10. The ICs packages like *single in-line* (SIP), *zigzag in-line* (ZIP) as well as *quad in-line* (QIP) are not as popular as DIP or PGA. *Transistor Outline Package* (TO) is commonly used for transistors and silicon-controlled rectifiers, but also for integrated circuits like linear voltage regulators (eg. LM78xx family).

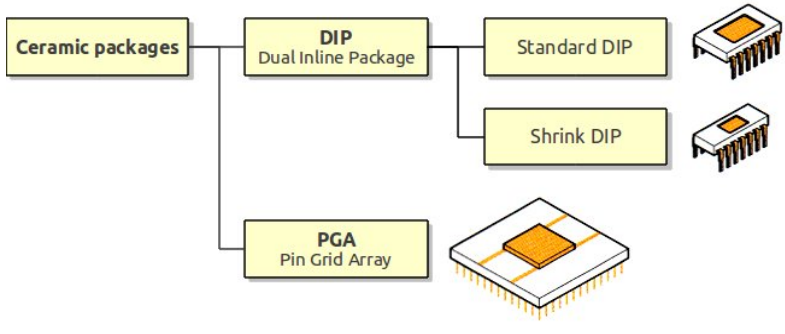


Figure 6.9 Through-hole ceramic IC packages (after Friedel K., [15])

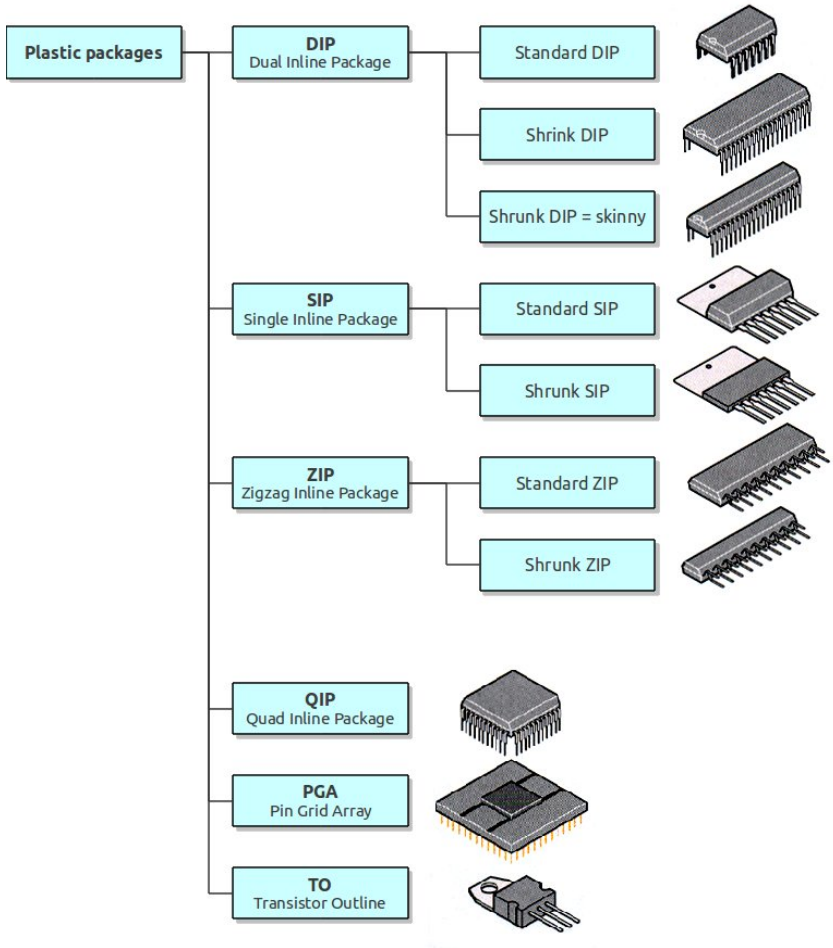


Figure 6.10 Through-hole plastic packages of ICs (after Friedel K., [15])

6.2. Surface-mount technology

Surface-mount technology (SMT) is a relatively new technology within electronic packaging, which has evolved from earlier technologies out of a strong desire and need for further miniaturization of electronic products with increased functional capability and reduced costs. Demand for smaller and smaller products with more and more functions at lower costs and increased reliability has resulted in SMT rapidly becoming the technology of choice for many of the new electronic products in the consumer, automotive, military, and telecommunication segments of the electronic industry. Because of this strong desire and need and its inherent advantages, the SMT is quickly moving into a more prominent role in the electronic industry [18].

SMT derives its name from the way its components (called SMC – *surface mount components* or SMD – *surface mount devices*) are attached to Printed Circuit Boards (PCBs). In SMT active and passive elements are repacked from solely leaded component packages, whose electrical and mechanical attachments depend on their leads being inserted and soldered in plated-through holes in the substrates, into packages whose electrical and mechanical attachments are dependent on solder joints oriented to surface mounting only [18].

There are two categories of surface-mounted terminations on SMT components, leaded and leadless. Device with terminations formed independent of, and projected away from, the component body are specified as leaded. Components with terminations formed as an integral part of the body are specified as leadless. The terms pin, lead, and terminal are often used interchangeably to refer to component terminations on the leaded as well as leadless SMT components [18].

6.2.1. Discrete devices

With very few exceptions, passive SMT components are leadless, that is, the terminations are formed on the surface of the components. Surface-mounted passive devices are available in a wide variety of package styles. The majority of passive devices used, however, are flat, rectangular shaped ceramic chip resistors and capacitors [18] or cylindrical shaped MELF (metal electrode leadless face) resistors and diodes.

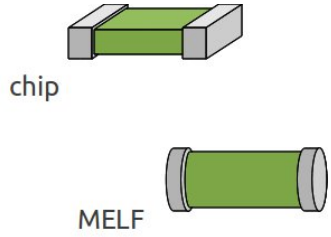


Figure 6.11 Chip vs. MELF packages

Chip resistors come in two basic types, thick-film and thin-film. Both are formed on alumina ceramic chips. Electrodes, serving as terminations, are formed on each end of the ceramic chip with the resistive element applied between them on the top surface of the ceramic substrate. The resistive element is made as screen printed ink or paste for thick-film types or as vacuum-deposited for thin-film types. Final adjustment of the resistance value is achieved by laser trimming a portion of the resistive element midway between the terminals. The resistive element is subsequently coated with a glass passivation to protect it from moisture and abrasive damage. Chip resistor terminals are generally formed as three-sided, electrically continuous wraparound pads from the bottom surface around the end to the top surface. This permits the formation of a fillet solder joint and exposes the resistive element for easy inspection [18].

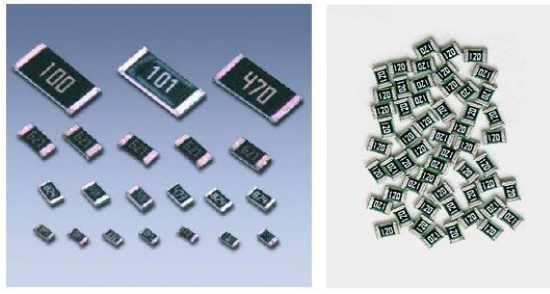


Figure 6.12 An example of SMD chip resistors

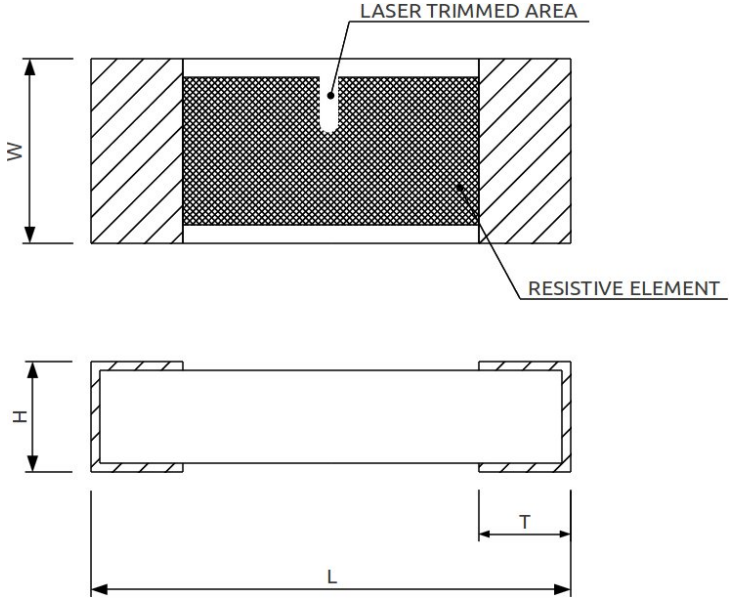


Figure 6.13 Standard Chip resistor (after Classon F.X. and Root J.A. [18])

*Tab*le *6.1:* Dimensions of selected standard SMD chip resistors

*Standard resistor number	Imperial [in]		Metric [mm]	
	*L	*W	L	W
0201	0.02	0.01	0.6	0.3
0402	0.04	0.02	1.0	0.5
0603	0.06	0.03	1.5	0.8
0805	0.08	0.05	2.0	1.2
1206	0.12	0.06	3.2	1.6
1210	0.12	0.10	3.2	2.5
1812	0.18	0.12	4.6	3.0

**Resistor numbers derived from L/W dimensions in inches.*

Other dimensions (height *H* and length of contact plate *T*) depend on power rating. Typical power ratings for some of the most popular SMD resistors are as follows:

- 1206: 1/8 Watt,
- 0805: 1/10 Watt,
- 0603: 1/16 Watt.

MELF (Metal Electrode Leadless Face) *resistors* are cylindrically shaped carbon-film and metal-film resistors. They are available in a wide variety of values and tolerances. These resistors are formed by coating the resistive element on alumina rods and applying electrodes as terminal caps on each end. Except for being leadless, they are very similar to conventional axial leaded resistors [18]. Besides the resistors, MELF packages are also used for diodes.

Figure 6.14 An example of SMD MELF resistors

Surface-mount *capacitors* were the first SMT devices used in large quantities in industry and still are even if no other SMT components are used. There are ceramic, tantalum, electrolytic, plastic, and mica capacitors. Ceramic capacitors, however, dominate the SMT industry. These devices are popularly known as ceramic chip capacitors [18].

Ceramic chip capacitors for SMT are basically constructed in the same way as their leaded counterparts. They consist of multilayered construction of ceramic sheets separated by metal films terminated at each end to form a monolithic structure. Unlike their earlier counterparts, however, they are not encapsulated in epoxy. Contrary to chip resistors, where a few standard sizes suffice for

a wide variety of values, the chip capacitor values and sizes are determined by the number and size of the interstructural dielectric layers. Higher voltage requires more layers and larger dimensions. Capacitance behavior over varying temperatures is another factor that governs ceramic capacitor construction and selection. Ceramic layers serve the dual function of structure and dielectric [18].

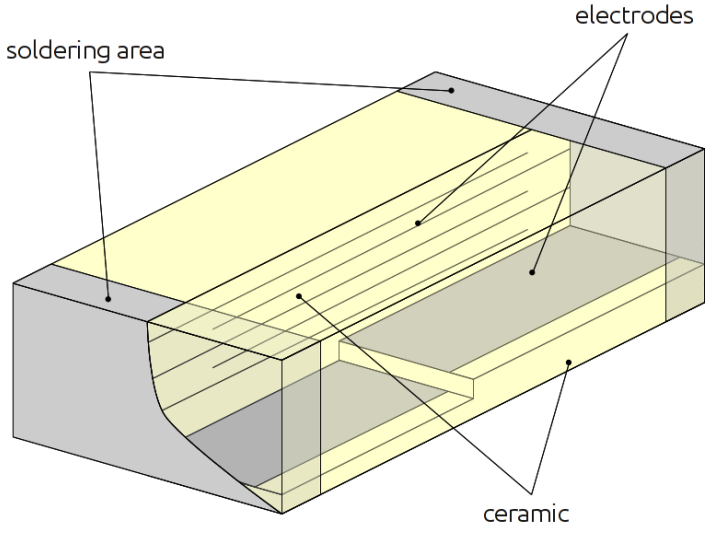


Figure 6.15 Typical ceramic chip capacitor construction

Solid tantalum chip capacitors are the next most often used chip capacitors. They apply when relatively high capacitance (1 to 300 μF) and small sizes are required.

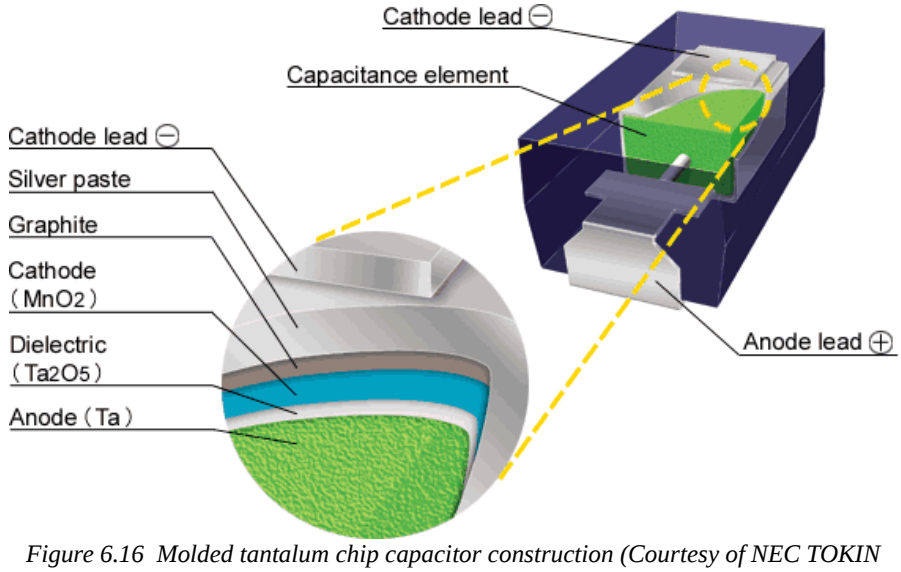


Figure 6.16 Molded tantalum chip capacitor construction (Courtesy of NEC TOKIN Corporation [19])

Figure 6.17 An example of molded SMD tantalum capacitor

Active components like diodes and transistors are also SMT made. SMD diodes come in a package body not unlike that of their leaded counterpart. It consists of leadless, cylindrical SOD (small-outline diode), MELF cases. SMT transistors are packaged in a nonhermetically sealed surface-mountable leaded molded plastic cases designated as an SOT-style package for small-outline transistors. The same package style has been expanded to include simple IC circuits, dual transistors, and light-emitting diodes (LEDs) [18].

6.2.2. Integrated circuits

SMT ICs come in a variety of package types. These package types are separated, depending on the form of leads, into peripheral packages (e.g. SOP, QFP, PLCC) and area array (e.g. BGA, fine pitch BGA). The surface-mounted IC packages are most often referred to as chip carriers.

SOP - Small Outline Package (see Figure 6.18) is similar in construction to the DIP (through hole, *Dual In-line Package;* see Figure 6.7) by using a copper leadframe for the pins, but the leads have minimal standoff, making it easier to use in a surface mount assembly process to attach to the circuit board. Unlike the plastic DIP, the thin SOP (or TSOP) is well-suited for packaging devices (like memory) in space constrained applications such as cell phones, notebooks, memory cards etc. When the package is fully encapsulated the TSOP is no greater than 1 mm in overall thickness [17].

Figure 6.18 An example of Small Outline Integrated Circuits

There are two different types of small outline packages: SOIC (*Small Outline Integrated Circuits*) and SOJ (*Small Outline J-lead package*). They differ in the shape of the pins. In SOIC package, the leads come out, down, and form a flat foot for securing to the board. They are referred

to as S-lead or gull-wing (see Figure 6.19, left). In SOJ package the pins bend under the package body like a letter "J" (J-lead, see Figure 6.19, right).

Figure 6.19 Different forms of SO leads: Gull-Wing leads (left) and J-leads (right)

The plastic *Quad Flat Pack – QFP* (Figure 6.20) is another established member of the family of peripherally-leaded packages like the SOP (and DIP) types. The main difference, however, from those packages is that the QFP leadframe runs around on all four sides of the package enabling higher pin counts, even up to 304 pins, although the most common usage ranges form 48 to 128. With the increasing demand for small and thin packages, the thin QFP or TQFP at 1 mm thickness is a very popular choice for lower cost microprocessors and other ICs for portable systems like laptops, wireless appliances, and so on. A ceramic QFP is preferred when resistance to high temperatures and humidity becomes an important design parameter [17].

Figure 6.20 304-pin QFP chip produced by SEGA (Courtesy of Wikimedia Commons)

Plastic Leaded Chip Carrier – PLCC (Figure 6.21) is a plastic, J-lead, four-sided IC package. PLCC package can be square or rectangular, and lead count ranges from 20 to 84. The PLCC “J” Lead configuration requires less board space versus equivalent gull leaded components, and is a less expensive version of the *Leadless Chip Carrier (LLCC)*, which is a housing with flat contacts instead of pin connectors, on each side.

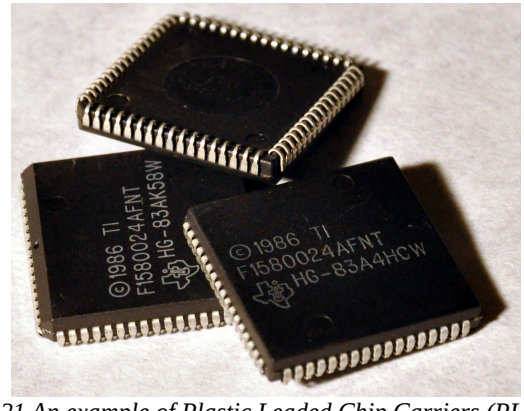


Figure 6.21 An example of Plastic Leaded Chip Carriers (PLCC)

A PLCC circuit may either be installed in a PLCC socket (Figure 6.22) or surface-mounted. The PLCC sockets may in turn be surface mounted, or use through-hole technology. The motivation to employ a surface-mount PLCC socket arises when the device cannot withstand the heat involved during the reflow process or to allow a component replacement without reworking. Using a PLCC socket may be necessary in situations where the device requires stand-alone programming, such as some flash memory devices.

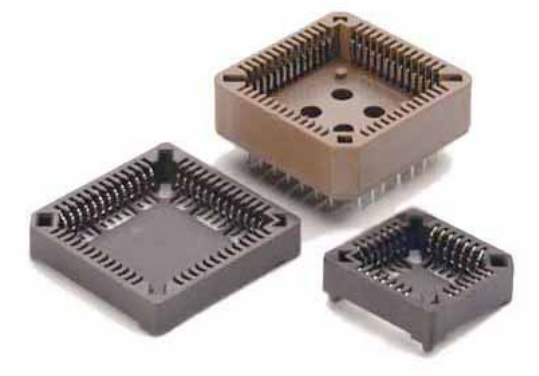


Figure 6.22 An example of PLCC Sockets (Courtesy of Andon Electronics [20])

In the late 1980s, packages with solder balls were developed as an alternative to packages with leads. The solder balls can be placed underneath the surface of the package in an area array and significantly increase the I/O count of surface mount packages. *Ball grid array* (*BGA*) is an example of this technology [2].

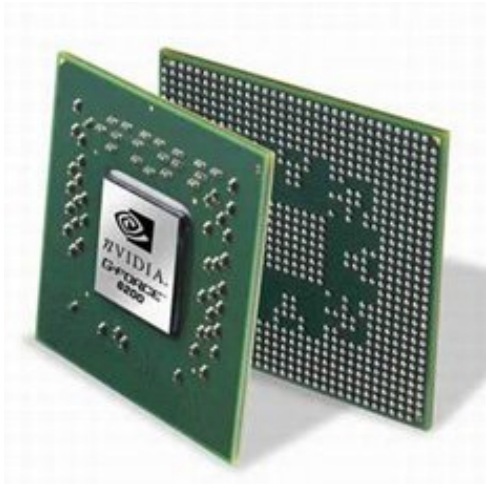


Figure 6.23 An example of BGA package – Nvidia GeForce GPU (Courtesy of Nvidia [21])

The size and performance limitations of peripherally-leaded packages like the QFP are completely overcome by the BGA package, which belongs to the new class of area array packages. The interconnect or terminals are formed by an array of solder balls located well within the boundaries of the package, unlike the leadframe connections used in DIPs, SOPs and QFPs. As the pin count grows, the size increase in the BGA package is much smaller compared to the QFP, so less space is also consumed on the circuit board for leading out the input/output pins.

There are three broad groups of BGAs: *plastic* (PBGA), *ceramic* (CBGA) and *tape* (TBGA), based on the materials used in constructing the substrate. For wirebond dies (Figure 6.24a) the PBGA is, by far, the package of choice when pin counts are in the 300 to 600 range. The TBGA package is chosen when low profile and improved electrical performance are required. The CBGA is used almost entirely for packaging of flip chip ICs (Figure 6.24b), most commonly in the 300 to 600 pin count range [17].

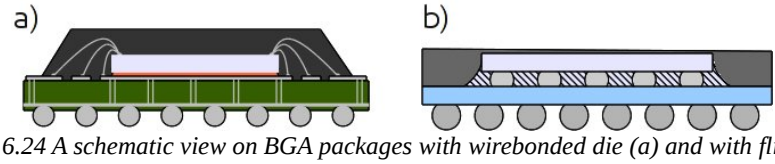


Figure 6.24 A schematic view on BGA packages with wirebonded die (a) and with flip-chip mounted die (b)

The plastic BGA has several advantages over most other single chip packages. These include [17]:

- **Size:** an area array of solder balls allows easy expansion of input/output terminals by increasing the I/O ball count while maintaining the I/O pitch.
- **Performance:** improved electrical and thermal performance due to the ability to include power and ground planes as part of BGA construction, the relatively short electrical interconnect path compared to lead frame packages, use of thermal vias, and heat sink attachments directly to the face of the die.

- **Easy to assemble:** to the *printed circuit board* (PCB) with the use of standard surface mount reflow processes. Board assembly defects are typically in the few tens of parts per million range, which can be two to five times better than in comparable fine pitch leadframe packages like TQFPs.

Leadless chip carriers LLCC (Figure 6.25) have a distinct advantage over the leaded carriers with regard to cost and packaging density, but their disadvantage is the short fatigue life of solder. Bare leadless packages, due to their relative simplicity and fewer materials, cost less than leaded packages. They do not have the handling, storage, assembly alignment, and coplanarity problems normally associated with the leaded packages. Some styles of leaded packages require larger land-pattern areas. The solder attachment of leadless devices, however, is rigid, with no mechanical compliant feature other than the solder joint itself to compensate for the stress caused by the mismatch in the coefficients of thermal expansion (CTEs) between the carrier and PWB. Stress forces increase as the carrier sizes and thermal cycles increase. Carrier size and lifelong thermal cycling, therefore, are major considerations in choosing between leaded and leadless devices. On the one hand, leadless devices should be chosen over the leaded ones every time when a maximum cost or packaging density advantage is to be gained. On the other hand, the component sizes and the system usage could be limited [18].

Figure 6.25 An example of Leadless Chip Carrier – LLCC (Courtesy of Analog Devices [22]*)*

The whole family of ceramic as well as plastic SMD packages is presented in Figure 6.26 and in Figure 6.27, respectively.

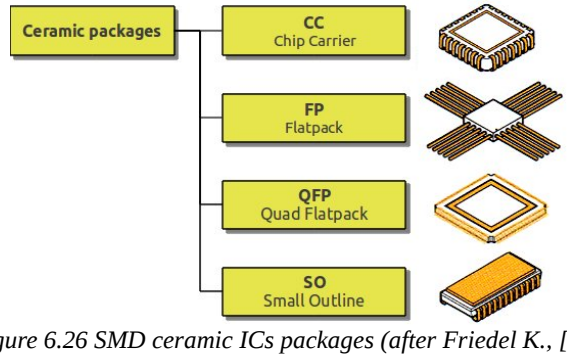


Figure 6.26 SMD ceramic ICs packages (after Friedel K., [15])

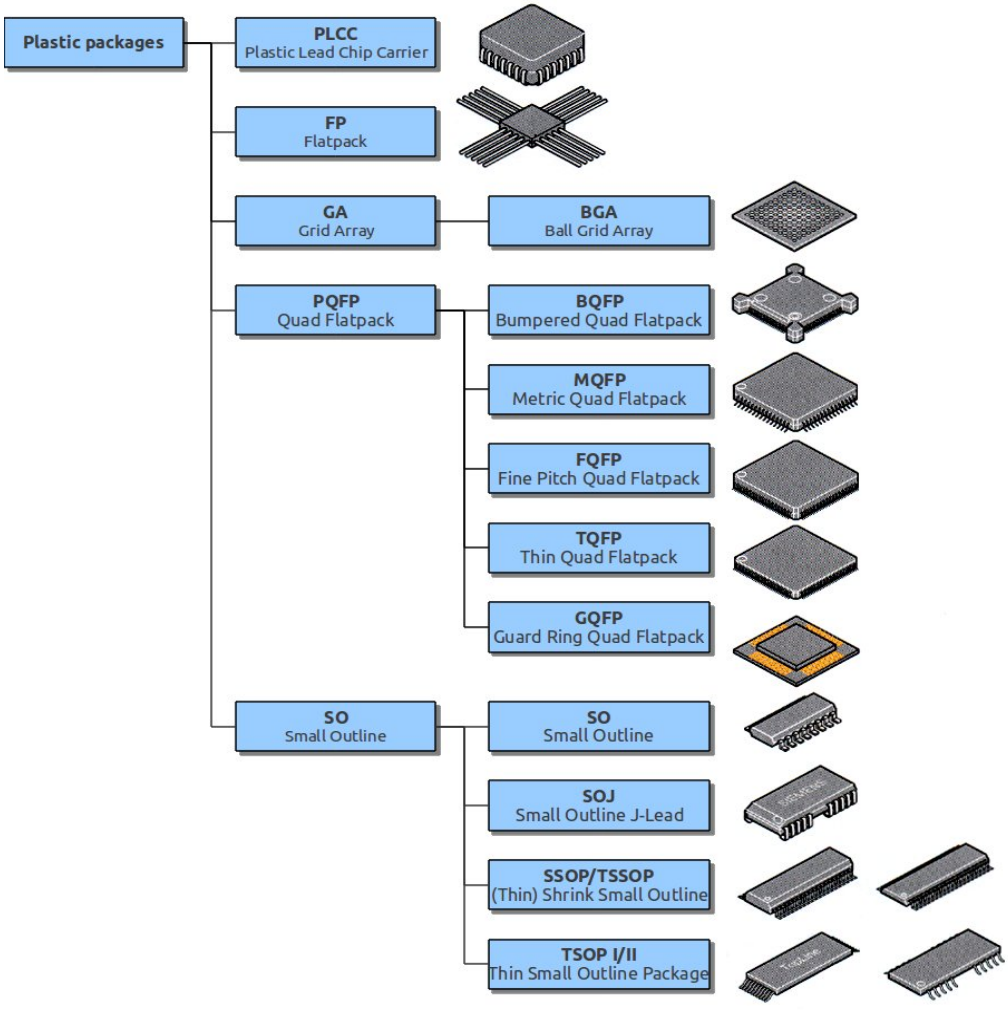


Figure 6.27 SMD plastic ICs packages (after Friedel K., [15])

7. Fundamentals of soldering process

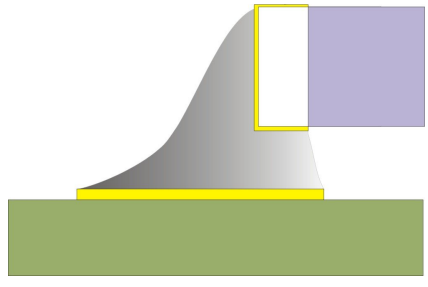
7.1. Soldering

The first historical mention of the soldering comes from 3000 B.C. The goldsmiths of ancient Egypt knew how to join gold. Tin was discovered as a soldering metal in 2000 B.C. Sumerians developed bronze (Cu90Sn10) in 300 B.C.

Soldering is a method of connecting metal elements using solder alloys with melting points lower than the melting points of connected elements. Solder alloys can be applied as the solid (reflow soldering) or molten alloys (wave soldering), while connected elements always remain solid. Soldering is used mostly in order to assembly of electronic components and integrated circuits on printed circuit boards (second level of assembly). The advantage of soldering is that the process is fully reversible. Therefore solder joints can be repaired without damage of substrates neither components [16].

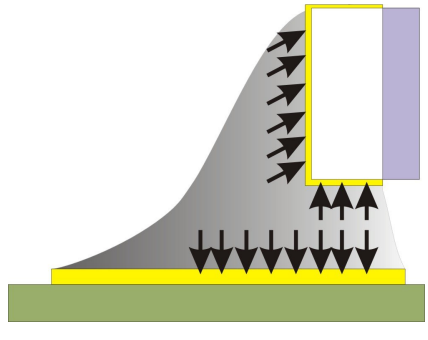
The following physical processes occur during soldering [16]:

- wetting of solder pads and leads of components with molten solder alloy,

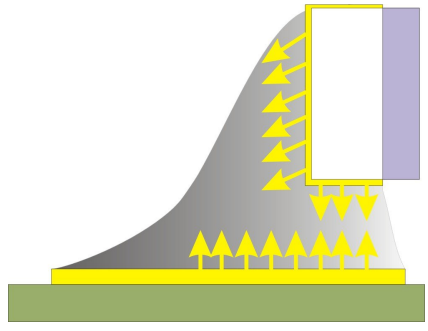


- filling of metallized holes and vias with molten solder as well as wetting of hole walls thanks to capillary forces,

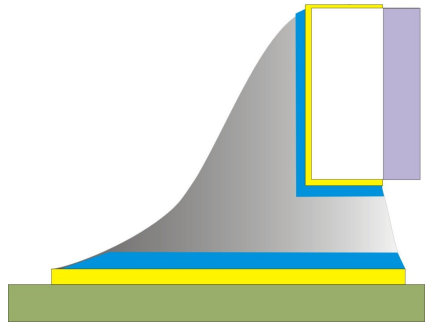
- diffusion of molten solder into the connected surfaces,



- dissolution of the substrate metals in solder joint,



- formation of intermetallic compounds at the boundary between solid (a solder pad or a component lead) and liquid (molten solder).



The processes depend on chemical composition of solder alloy and joined metals, the duration of the reactions as well as the temperature of molten solder. Moreover the efficiency of both wetting and filling with solder alloys depends on chemical composition of the applied flux. Solder joints solidify during cooling after the soldering process. Despite the fact that the solidification stops further dissolution of substrate metals in the solder, interfacial reactions can remain in the solid. The interfacial reactions in solid run much slower than in liquid because the temperature is much lower as well as diffusion processes run much slower in solid than in liquid. Diffusion in solid leads to formation of one or more intermetallic layers [16].

7.2. Materials for soldering

According to McGraw-Hill Science & Technology Encyclopedia term “alloy” is generally applied to any homogeneous molten mixture of two or more metals, as well as to the solid material that crystallizes from such a homogeneous liquid phase. Alloys may also be formed in solid-state reactions. In the liquid phase, alloys are essentially solutions of metals in one another, although liquid compounds may also be present. Solid alloys may vary greatly in range of composition, structure, properties, and behavior [23].

Solder alloys can be delivered as:

- solder wires as presented in Figure 7.1 [24],

- solder paste as presented in Figure 7.2 [25],
- solder bars as presented in Figure 7.3 [26].

Solder paste consists of solder alloy (65-96% weight) and flux. The diameter of solder paste particles is:

- 20-38 μm in case of ultra fine pitch (<380 μm),
- 25-45 μm in case of fine pitch (380 – 630 μm),
- 45-78 μm in case of standard pitch (640 - 1270 μm).

Figure 7.1 Wire spools of solder alloy [24]

Figure 7.2 Solder alloy paste [25]

Figure 7.3 Solder alloy bars [26]

7.3. Solder wetting

Durability of a solder joint depends mostly on the coverage of connected surfaces with the solder alloy. It is related to the wetting properties of the solder alloy. Solder wetting is an ability to cover the connected surfaces with thin, uniform and continuous coating of solder. If the surfaces are well cleaned and not re-oxidized then one can assume that three elements take part in the soldering process: solder, substrate metals and atmosphere of soldering (air or vapor fluxes). At the soldering temperature the substrate metals remain solid, the molten solder remains liquid and the flux becomes a gas [16].

The substrate metals are well wetted with the molten solder if the forces of mutual attraction between the molecules of molten solder and molecules on the surface of substrate metals are greater than cohesion strength between the molecules of molten solder. In conditions of thermodynamic equilibrium the soldering can be considered as a system of three phases: solid, liquid and vapor [16]. Figure 7.4 shows the thermodynamic equilibrium diagram of wetting during soldering process where:

$\vec{\gamma}_{LV}$ - surface tension between molten solder and vapor phase,

$\vec{\gamma}_{SV}$ - interfacial tension between substrate metal and vapor phase,

$\vec{\gamma}_{LS}$ - interfacial tension between molten solder and substrate metal.

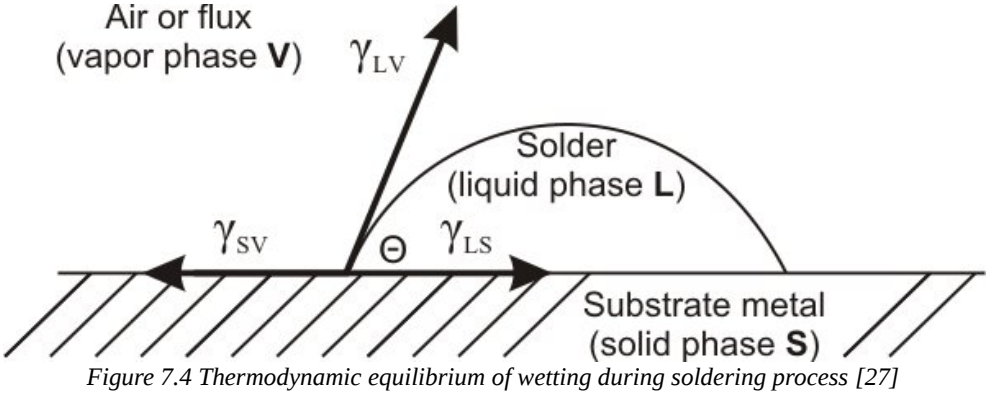


Figure 7.4 Thermodynamic equilibrium of wetting during soldering process [27]

Surface tension is a property of a surface of a liquid that allows it to resist an external force. Surface tension has the dimension of force per unit length or of energy per unit area. The phenomenon of surface tension is connected with the cohesive forces among the liquid molecules.

Within the bulk of the molten solder, each molecule is pulled equally in every direction by the neighboring liquid molecules, resulting in a zero net force. The molecules at the surface do not have other molecules on all sides of them and consequently are pulled inwards. Figure 7.5 shows a diagram of the forces on molecules of molten solder.

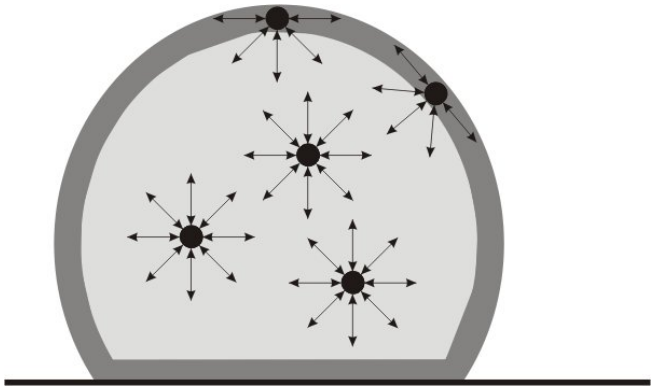


Figure 7.5 Diagram of the forces on molecules of molten solder

The phenomenon creates some internal pressure which the forces surface of molten solder to shrink to the minimal area. Moreover, the surface tension is responsible for the shape of molten solder droplets. The higher surface tension, the more spherical shape of the droplet.

Thermodynamic equilibrium is described by the Young's equation:

$$\vec{\gamma}_{SV} + \vec{\gamma}_{LS} + \vec{\gamma}_{lV} = 0 \,.$$

The position of both $\vec{\gamma}_{SV}$ and $\vec{\gamma}_{LS}$ vectors of interfacial tension is along substrate metal, but their directions are opposite. On the basis of the diagram of thermodynamic equilibrium presented in Figure 7.4, one can obtain the following formula where γ_{SV} is the wetting force:

$$\gamma_{SV} = \gamma_{LS} + \gamma_{lV} \cos(\theta) \,.$$

If the θ angle is 180°, wetting does not occur as presented in Figure 7.6, if the θ angle is 0° total wetting occurs as presented in Figure 7.7, if the θ angle is between 0° and 180° partial wetting occurs, according to the Figure 7.8.

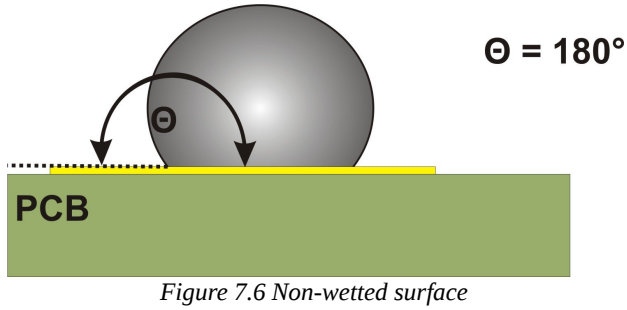


Figure 7.6 Non-wetted surface

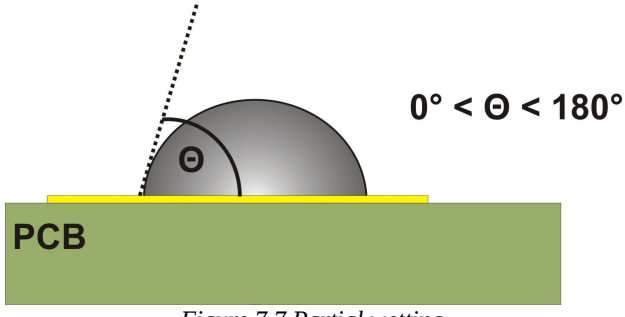


Figure 7.7 Partial wetting

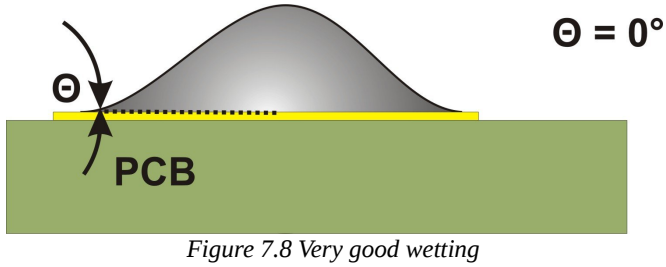


Figure 7.8 Very good wetting

Because of too short duration of soldering process and immediate cooling phase (in order to solidify the molten solder), thermodynamic equilibrium is very rare condition. In practice it is assumed that poor wetting occurs when the θ angle is between 90° and 75°, good wetting is obtained when the θ angle is less than 75°. When high quality of solder joint is required the θ angle should not exceed 55°. The best wetting is obtained when the θ angle is between 0° and 25°.

Solder wetting depends mostly on cleanness of soldered components. Contamination of oxides, grease and salts may increase the θ angle. In order to reduce the θ angle fluxes are used. Wettability is commonly evaluated using meniscograph. It is difficult to measure the θ angle precisely, therefore, the force and wetting duration are measured during evaluations.

7.4. Fluxes and their role in soldering

Fluxes are necessary to carry out a proper joint. Fluxes do not create a connection and are not incorporated in the connection. Fluxes fulfill three functions:

- remove oxide film and other contamination from the surface of soldered surfaces and the liquid solder,
- molten film of flux protects heated area of solder joint against chemical reaction of the surrounding gas,
- reduce surface tension of molten solder.

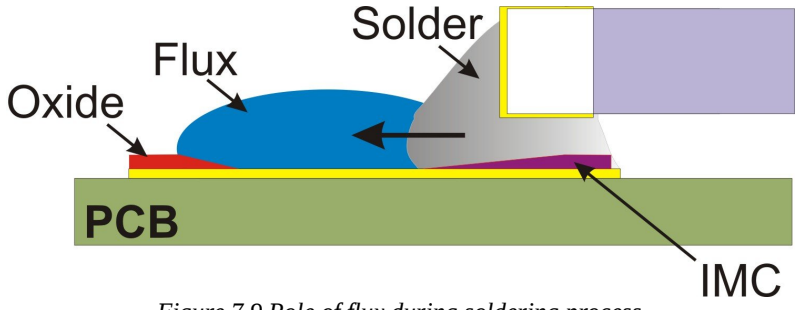


Figure 7.9 Role of flux during soldering process

Main requirements on fluxes are:

- melting point of flux should be lower than melting point of solder alloy,
- evaporating temperature should be higher than evaporating temperature of solder alloy,
- at soldering temperature flux should be sufficiently liquid in order to melt on the surface uniformly, and easily penetrate into the slots,
- chemical inertia with respect to joined metals and solder alloy,
- flux should dissolve non-metallic compounds from the surface of joined metals and solder alloy,
- flux should protect solder joint against the harmful influence of gases,
- mutual attraction between flux and metal should be less than mutual attraction between metal and flux,
- flux should not change its chemical composition during heating,
- flux residuals and molten non-metallic compounds should flow to the surface when molten solder alloy touches metal,
- flux residuals should be easily removable from the surface of solder joint,
- flux should not change its chemical composition during storage,
- flux should not contain harmful, expensive and deficient substances,
- flux should not release harmful gases.

Most popular fluxes are:

- rosin-based fluxes,
- “no clean” fluxes,
- water-based “VOC-free” fluxes.

Rosin-based fluxes consist of colophony, activator and solvent. Colophony is solid in room temperature and becomes liquid when heated to 125-150°C. The main component of colophony is abietic acid ($C_{20}H_{30}O_2$) that partially dissolves copper and tin oxides. Solvent is a carrier for other ingredients, it is usually isopropyl alcohol.

Fluxes, which are based only on colophony are fluxes of low activity. Such fluxes are marked as “R”. In order to increase activity, activators (such as halides) are added. Activators react strongly with contamination at high temperature. Depending on the amount of activator, fluxes are marked as “RMA” (mildly activated), “RA” (activated) and “RSA” (strongly activated). The residues (a substance deposited or left after soldering process) can be electrically conductive or corrosive. It is strongly recommended to remove the residues of fluxes after the soldering process.

Nowadays fluxes which do not require removal become very popular. Such fluxes contain less than 40% of colophony and are called “no-clean” fluxes. At high temperature organic molecules polymerize and harden blocking access to oxygen and moisture. The residues are not corrosive and do not have to be removed.

Water-based fluxes contains water instead of volatile organic compounds, therefore are called “VOC-free”. VOC-free fluxes are non-flammable in opposite to the fluxes which contain organic solvents.

7.5. Intermetallic compounds

According to McGraw-Hill Science & Technology Encyclopedia intermetallic compounds are materials composed of two or more types of metal atoms, which exist as homogeneous, composite substances and differ discontinuously in structure from that of the constituent metals.

In the literature intermetallic compounds are also often called intermetallic phases. The properties of IMCs can not be transformed continuously into those of their constituents by changes in composition alone, and they form distinct crystalline species separated by phase boundaries from their metallic components and mixed crystals of these components. It is generally not possible to establish formulas for intermetallic compounds on the sole basis of analytical data, so the formulas are determined in conjunction with crystallographic structural information [23].

In case of solder joints the most common intermetallic compounds are Cu_3Sn, Cu_6Sn_5, Ag_3Sn and $AuSn_4$. Depending on the constitution the IMCs can be located in the bulk of solder joint or along the boundary between the solder joint and metallization (component metallization or solder pad metallization). Some examples of IMCs in different locations are presented in Figure 7.10 and in Figure 7.11 [27].

The intermetallic compounds are formed during alloy solidification as well as after soldering process during solid-phase diffusion. In case of intermetallic compounds, metallic bonds dominate, but also ionic as well as covalent bonds can be present.

Major reliability problems with intermetallic phases are void formation and excessive growth of intermetallic compound layers caused by excessive diffusion of metals between the layers. Both Kirkendall voids and brittle layers of Cu_3Sn, Ni_3P or Ni_3Sn can reduce the strength of a solder joint. Intermetallic phases used to be harder than solder alloys, therefore solder joints that contain thin homogeneous, uniform layers of IMCs crack easily when subjected to tension.

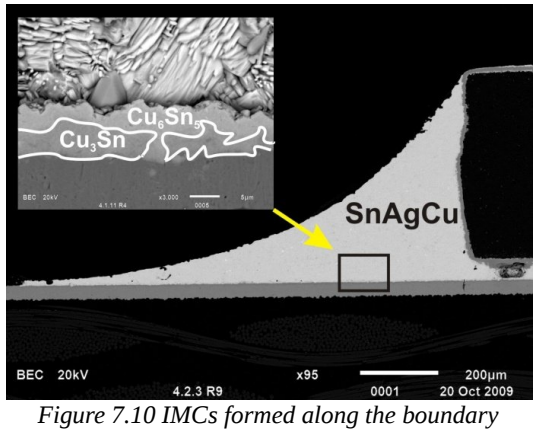


Figure 7.10 IMCs formed along the boundary between a solder joint and pad metallization [27]

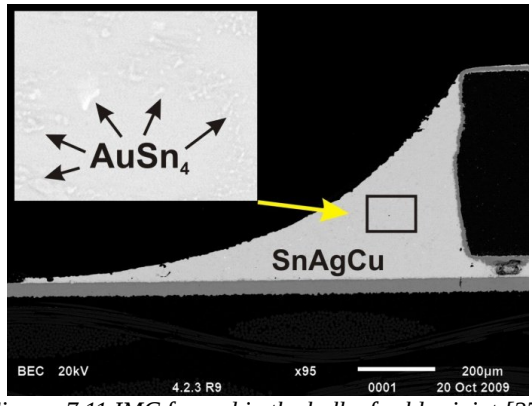


Figure 7.11 IMC formed in the bulk of solder joint [27]

Thickness of an intermetallic compound layer is a function of temperature and time. The thickness can be calculated from the equation:

$$Y = Y_0 + \sqrt{Dt} \quad ,$$

where:

D- diffusion coefficient.

Diffusion coefficient can be calculated from the equation:

$$D = D_0 e^{(-\frac{Q}{RT})} \quad ,$$

where:

Q- activation energy.

Constitution of intermetallic compounds depends on metals that diffuse to solder alloy according to the following table.

Components		IMCs
Lead-free alloy	Cu	Cu_3Sn, Cu_6Sn_5, Cu_4Sn
	Ni	Ni_3Sn, Ni_3Sn_4
	Ag	Ag_3Sn
	Au	$AuSn_4$, AuSn

7.6. RoHS Directive

According to the European Directive 2002/95/EC RoHS which was adopted in February 2003 by the European union and took effect on 1 July 2006 the member states have to restrict the use of the following six substances in electrical and electronic equipment:

- lead (Pb),
- mercury (Hg),

- cadmium (Cd),
- Hexavalent chromium (Cr^{6+}),
- Polybrominated biphenyls (PBB),
- Polybrominated diphenyl ether (PBDE).

Both polybrominated biphenyls and polybrominated diphenyl ether are flame retardants used in several plastics. The directive applies to equipment as defined by a section of the WEEE directive (on waste electrical and electronic equipment). The following numeric categories apply:

- large and small household appliances,
- IT equipment,
- telecommunications equipment,
- consumer equipment,
- lighting equipment – including light bulbs,
- electronic and electrical tools,
- toys, leisure and sports equipment,
- automatic dispensers.

7.7. Materials complied with RoHS Directive

The European regulations took effect mostly on the assembly technology of electrical and electronic equipment. Since the beginning of the development of electronic assembly technology SnPb solder alloys have been used. Nowadays solder alloys which contain lead have to be replaced with lead-free equivalents. Lead as a component of solders had to be replaced by other metals, such as copper, silver or gold. Replacing the well-known technology that had been utilized for many years with a new technology (that bases on lead-free solders or electrically conductive adhesives) results in technological problems as well as in reliability problems.

Technological problems such as higher soldering temperature were easy resolved by adapting soldering equipment and materials to soldering in higher temperature. In fact the assembly process had to be modified because soldering lines had to be adapted to perform the process in higher temperature (the reflow temperature of lead-free alloys is on the average 40°C higher than the reflow temperature of eutectic SnPb solder alloys). Lead-free solder alloys for wave and reflow soldering recommended by global consortia are presented in table 7.1.

As well as production lines also constitution of pad coatings and fluxes had to be adapted to new lead-free alloys. Among solder pad coatings the most popular for lead-free soldering are ENIG (Electroless Nickel Immersion Gold) and ImSn (immersion tin), HASL (Hot Air Soldering Level). It is recommended to use water-based fluxes for lead-free soldering.

High coplanarity and resistance to oxidation are the main advantages of electroless nickel immersion gold coatings. The main disadvantages of ENIGs are high cost and black pad effect that can reduce mechanical strength of a solder joint significantly.

Table 7.1: Lead-free solders recommended by global consortia [27]

Technology / Consortium	Wave soldering	Reflow soldering
SOLDERTEC	SnAg3,8Cu0,25 **(217÷223°C)**	SnAg3,8Cu0,7 **(217÷223°C)**
IDEALS	SnAg(3,4-4,1)Cu(0,45-0,9) **(217÷223°C)**	
JEITA	SnAg3,0Cu0,25 **(217÷223°C)**	
NEMI	SnCu0,7 **(227°C)**	SnAg3,9Cu0,6 **(217÷223°C)**

Main advantages of immersion tin are low price and coplanarity, the main disadvantages are oxidation and tin whisker growth.

Hot air solder leveling coatings are low cost and low coplanarity coatings, therefore are not used in case of small outline integrated circuits. All investigated pad coatings are well wetted by molten solder, if not oxidated.

7.8. Reliability problems of lead-free solder joints

Replacing the well-known materials with the new ones not only forces technological adaptations but also imposes necessity of reliability investigations, especially of new failure modes. New material compositions caused changes within a solder joint structure e.g. new intermetallic compounds (IMCs), more defects such as Kirkendall voids, microcracks, gas pores. In fact, in spite of years of investigations and modifications, lead-free solder joints are much less resistant to mechanical loading and fatigue failures than lead-based solder joints. Lead-free solder joints subjected to outer mechanical or environmental loadings crack easily. Fatigue cracks occur within the joint when it is subjected to vibrations or thermal cycling. Examples of solder joint cracks are presented in Figure 7.12 and in Figure 7.13.

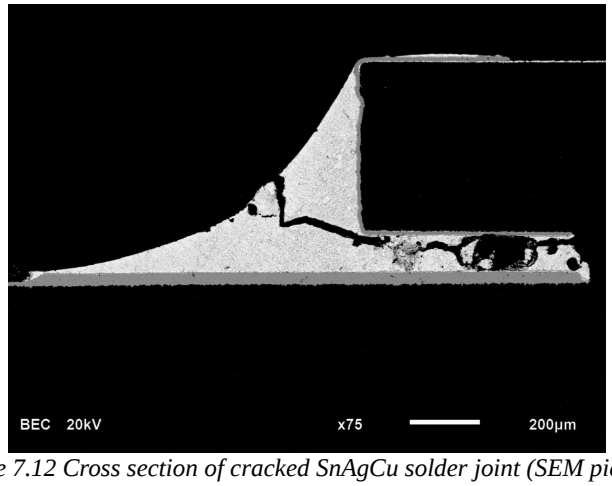


Figure 7.12 Cross section of cracked SnAgCu solder joint (SEM picture)

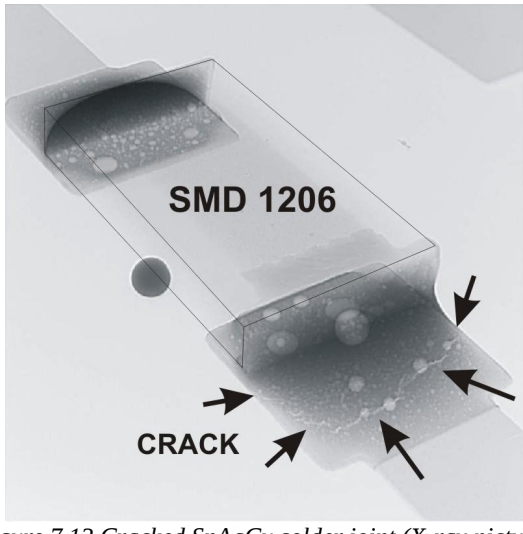


Figure 7.13 Cracked SnAgCu solder joint (X-ray picture)

The other problem of lead-free solder joints especially in case of ImSn pad coatings joints are tin whiskers. A whisker is a single crystal that grows spontaneously from a surface of a pure metal.

Apart from tin, whiskers can also be a single crystal of tin, indium, cadmium, zinc, gold, silver, lead. Whiskers are typically 1 μm in diameter but can grow to, the length from 10 μm up to 10 mm. Tin whiskers that have grown from tin-copper coated lead-frame are presented in Figure 7.14 [28].

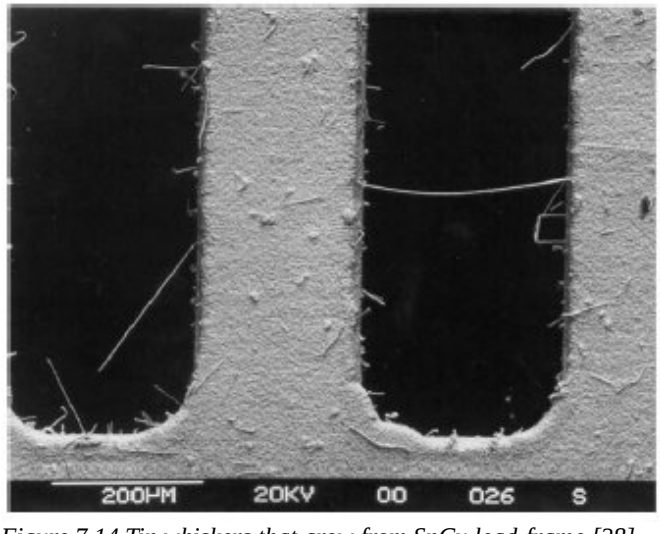


Figure 7.14 Tin whiskers that grow from SnCu lead-frame [28]

Whiskers can grow as kinked, bent, striated, needle (filament) or may take odd shape. Examples of whisker shapes are presented in Figure 7.15.

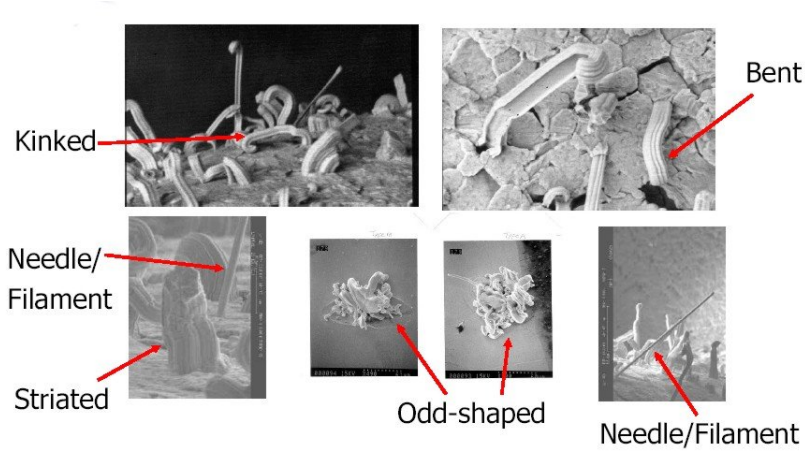


Figure 7.15 Different shapes of whiskers [28]

The whiskers growth is a problem of Pb-free solders. Nevertheless the whiskers also occur in case of Pb solders but the phenomenon is very rare. The reason, why the phenomenon of whisker growth is so common in case of Pb-free solder joints, hasn't been completely understood yet. The crucial observation that may help to understand the mechanism of the growth is that the whiskers have a nature of screw dislocation.

It's known that phenomenon is triggered by the interaction between Cu, Sn thin films and IMC that is formed along the interfacial region. The whiskers can grow with and without electrical field both in vacuum and atmosphere. The most rapid growth can be observed at 50°C. This is the temperature of tin recrystallization. Rapid growth was also observed in the range from the room temperature to 75°C.

Growth rate is rather unpredictable, it may take few days as well as few years. Main factors that trigger whiskers growth are stresses, both internal and external. The stresses may be caused by grain size, shape and orientation in case of pure metal film, by irregular thick and fast formation in case of IMC, by interaction between substrate, metal film or IMC and finally by bending, scratching and thermal cycling.

The whiskers are able to decrease reliability of electronic devices in two ways. The first one is an electric failure, the other one is a mechanical failure. First of all, the whiskers are electrically conductive and may trigger transient or permanent shorts. It depends on conducted current. If the current is less than 10 mA the short is permanent, unless is transient. The whiskers can also generate debris and contaminates, that can interfere with sensitive optics or MEMS and affect failures.

8. Overview of soldering technologies

Depending on the size of series and design of printed circuit board we can apply:

- reflow soldering,
- wave soldering,
- manual soldering.

Depending on soldered components we can distinguish:

- surface mount technology (SMT) in case of surface mount devices (SMD).
- through-hole technology in case of through hole devices (THD).

8.1. Difference between reflow and wave soldering

The main difference between reflow soldering technology and wave soldering technology is the way to deliver heat and solder alloy. In case of reflow soldering solder paste is deposited during one process and the heat is delivered during other process. In case of wave soldering the molten solder and heat are delivered during one process. Schematic of wave and reflow soldering are presented in Figure 8.1.

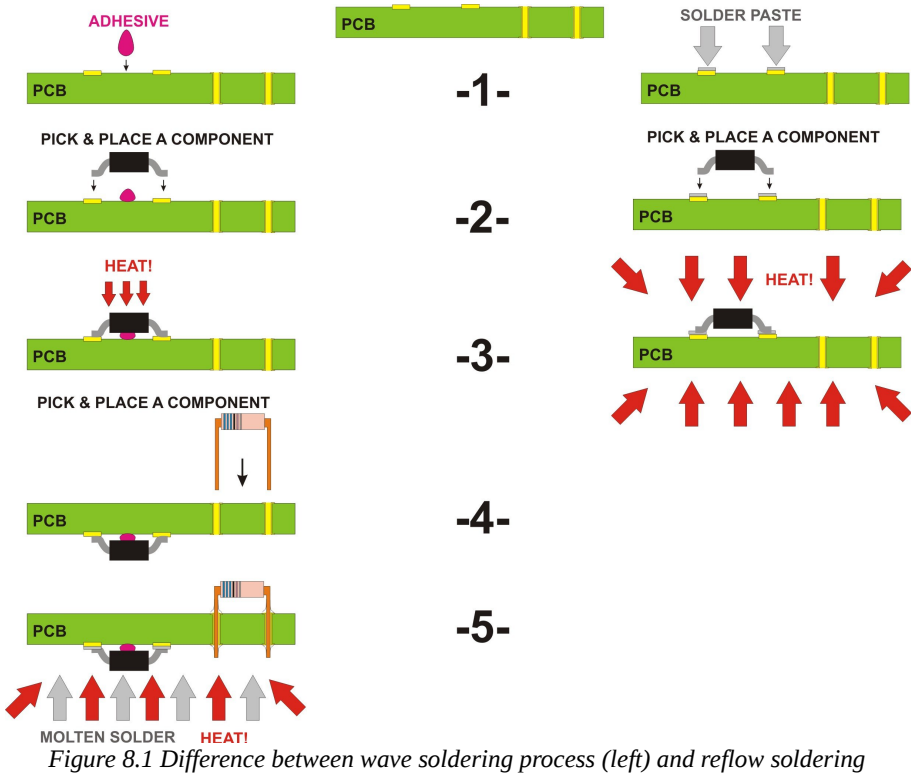


Figure 8.1 Difference between wave soldering process (left) and reflow soldering technology (right)

According to the Figure 8.1 the reflow soldering is less complicated process than the wave soldering especially in case of SMD components (three stages instead of five processes for wave soldering). In case of SMD components and wave soldering we need to fix the components to the surface of PCB using epoxy resin before the proper soldering process.

8.2. Application of soldering technologies

One sided PCBs can be soldered during reflow soldering process or wave soldering process. According to Figure 8.2. the reflow soldering must be preceded by stencil printing of solder paste and pick and place of components.

Figure 8.2 One sided PCB with SMD components prepared for reflow soldering

According to Figure 8.3 before wave soldering an adhesive must be applied, then the components must be picked and placed, the adhesive must be curred, and finally the PCB must be inverted.

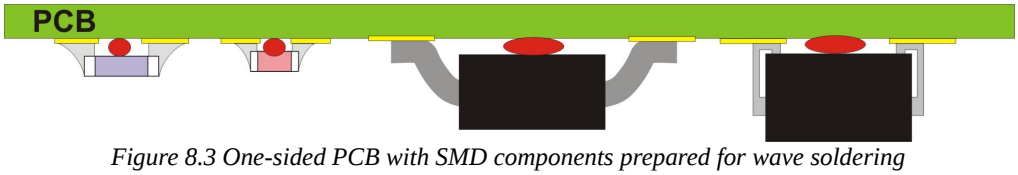


Figure 8.3 One-sided PCB with SMD components prepared for wave soldering

When PCBs are both sided as presented in Figure 8.4. We can apply two wave soldering processes. Such procedure consists of:

- applying an adhesive,
- pick and place components,
- curing the adhesive,
- inverting the PCB,
- wave soldering,
- applying the adhesive,
- pick and place components,
- curing the adhesive
- inverting the PCB,
- through hole assembly,
- wave soldering.

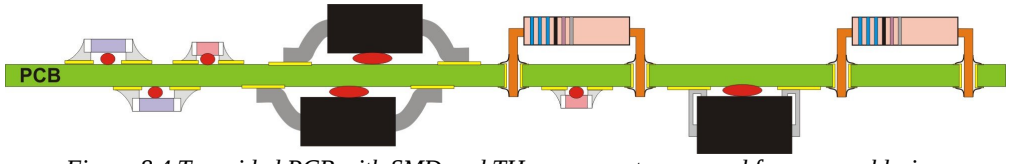


Figure 8.4 Two-sided PCB with SMD and TH components prepared for wave soldering

Two-sided PCBs can be also soldered using reflow soldering processes. PCBs such as presented in Figure 8.5 can be soldered during two reflow soldering processes and manual soldering process. Such procedure consists of:

- stencil printing of solder paste,
- pick and place components,
- reflow soldering,
- inverting the PCB,
- stencil printing of solder paste,
- pick and place components,
- reflow soldering,
- manual soldering.

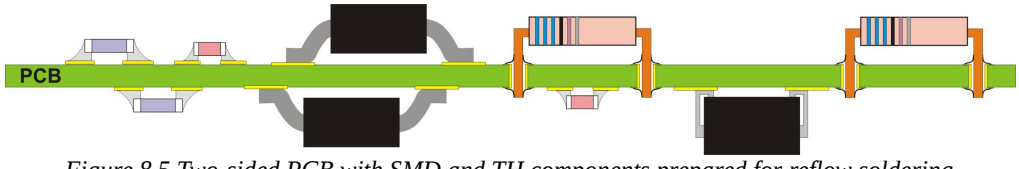


Figure 8.5 Two-sided PCB with SMD and TH components prepared for reflow soldering

Two-sided boards as presented in Figure 8.5 which can be also soldered using both reflow and wave soldering process. Such procedure consists of:

- stencil printing of solder paste,
- pick and place components,
- reflow soldering,
- inverting the PCB,
- applying an adhesive,
- pick and place components,
- curing the adhesive,
- stencil printing of solder paste,
- inverting the PCB,
- through-hole assembly,
- wave soldering.

Multiple reflows affect the structure of solder joints(especially thickness, and constitution of intermetallic compounds), but do not affect mechanical strength of solder joint significantly [29]. The thickness and constitution of intermetallic compounds affects fatigue resistance of solder joints [27].

The choice of technology depends on PCB design, kind of components and available equipment for soldering.

8.3. Equipment for manual soldering

Manual soldering is still very important process in case of mounting of electronic devices. It can be the sole and the core technology of soldering in case of atypical components or any other components that can not be assembled in an automated process (wave of reflow soldering). Manual soldering is also applied for improvements and repairs of mounted PCBs.

Basic equipment for manual soldering is presented in Figure 8.6.

Figure 8.6 Basic equipment for manual soldering (Courtesy of producers, source: Google Image)

We can distinguish:

- soldering gun and pot,
- rework station,
- “third hand” soldering station,
- analog soldering station,
- hot air rework station.

Other helpful equipment for manual soldering presented in Figure 8.7 is:

- solder remover,
- fan fume absorber benchtop,
- cleaning sponge,
- magnifying glass ring,
- BGA reballing stencils,
- pliers,
- tweezers.

Figure 8.7 Other helpful equipment for manual soldering (Courtesy of producers, source: Google Image)

In addition to the equipment listed above, the following materials are used:

- solder alloys (wires and solder paste),
- reballing balls (for ball grid arrays (BGA) packages),
- fluxes (liquid, flux pen or colophony resin).

8.4. Equipment for reflow soldering

In the reflow process a solder joint is formed during melting of solder alloy balls contained in solder paste. The solder paste is deposited by screen printing. The paste is deposited on the solder pads of PCB. PCBs with components placed on solder pads pass through reflow oven. The reflow oven delivers heat directly to the PCBs. The flux contained in the solder paste dissolves contaminations. The solder paste reaches the temperature of soldering. The example of a temperature profile of reflow soldering of SnPb is presented in Figure 8.8 [30].

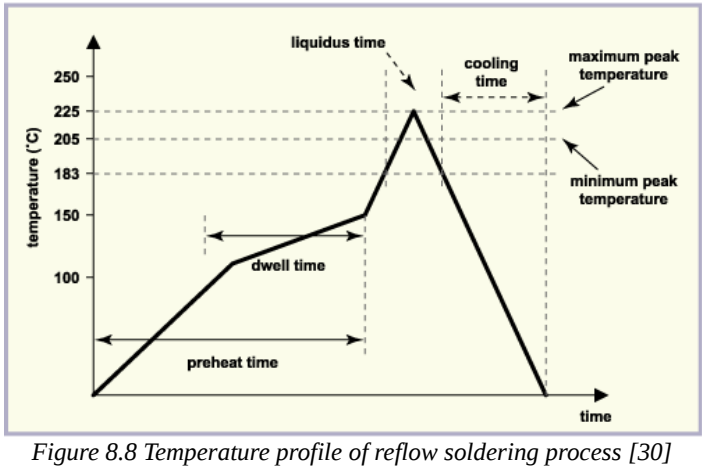


Figure 8.8 Temperature profile of reflow soldering process [30]

According to the figure 8.9, the reflow soldering line consists of [31]:

- stencil/screen printer,
- solder paste inspection unit,
- pick and place machines,
- automatic optical inspection unit,
- reflow process inspection unit,
- reflow oven.

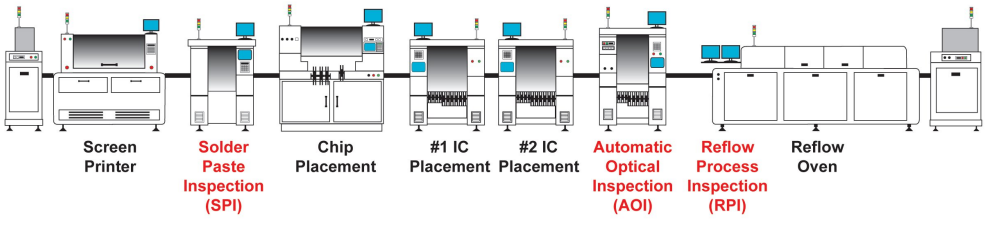


Figure 8.9 Reflow soldering line [31]

Multi-zone reflow oven for reflow soldering is presented in Figure 8.10 [32].

Figure 8.10 ERSA reflow oven for reflow soldering [32]

Process flow of reflow soldering is presented in Figure 8.11 [27].

The variety of reflow soldering that support multi-zone reflow in ovens are:

- vapor phase soldering,
- soft beam soldering,
- laser soldering,
- hot gas and hot-bar soldering.

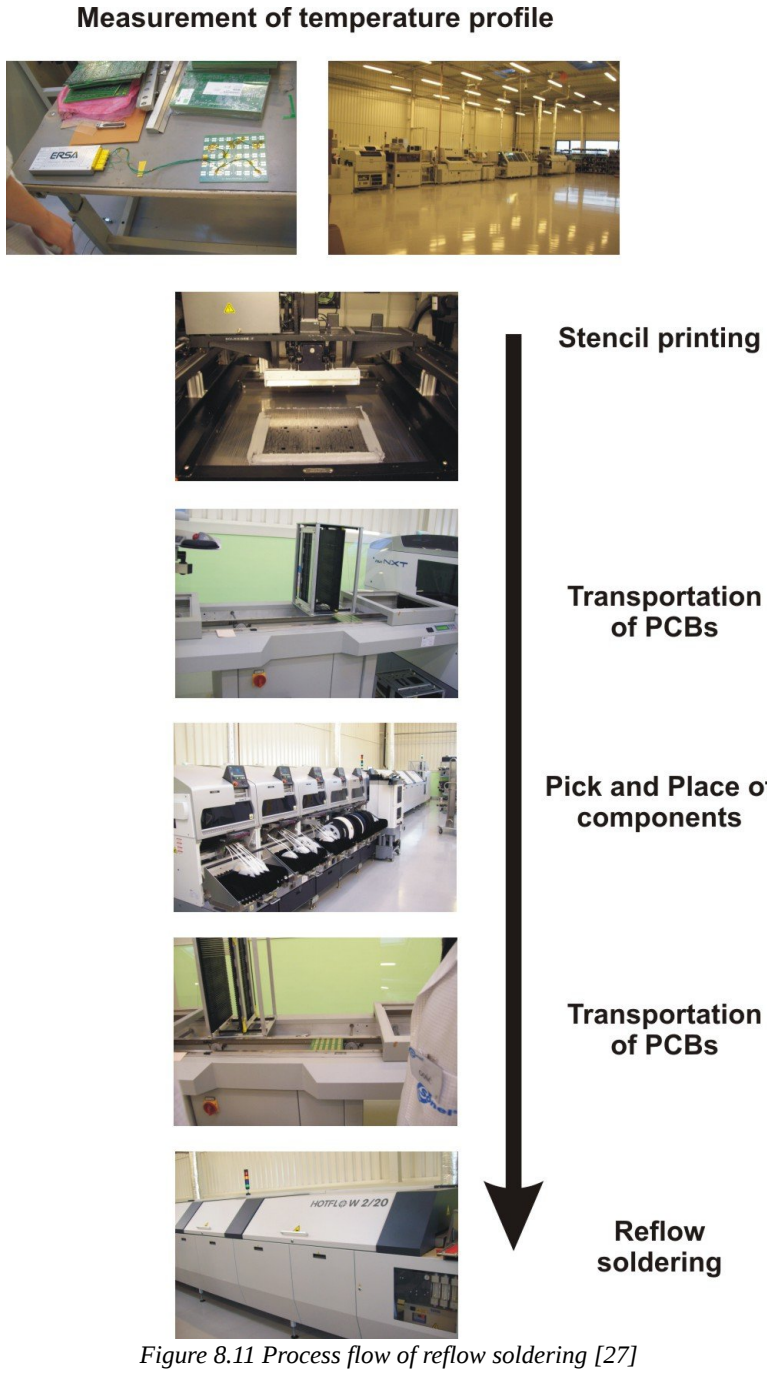


Figure 8.11 Process flow of reflow soldering [27]

8.5. Equipment for wave soldering

In case of wave soldering a stationary wave of molten solder alloy is used. The wave is supplemented continuously by fresh alloy from the bottom of the bath. PCBs with components attached using epoxy resin pass above the flux zone, preheating zone and across the wave of molten solder (soldering zone). Schematic of the wave soldering process is presented in Figure 8.12.

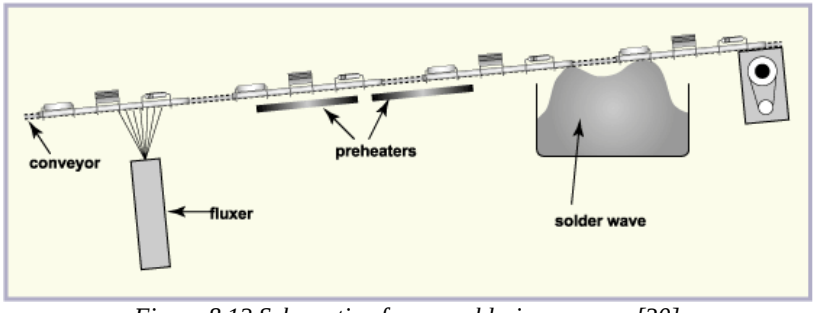


Figure 8.12 Schematic of wave soldering process [30]

Flux can be deposited using:

- foam fluxer,
- wave fluxer,
- spray fluxer.

Different fluxing methods are presented in Figure 8.13.

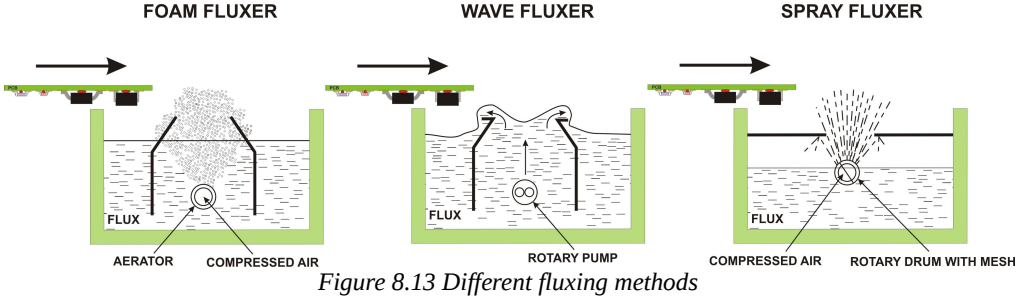


Figure 8.13 Different fluxing methods

Depending on the solder wave system we can distinguish:

- single wave systems ('T'wave) as presented in Figure 8.14.

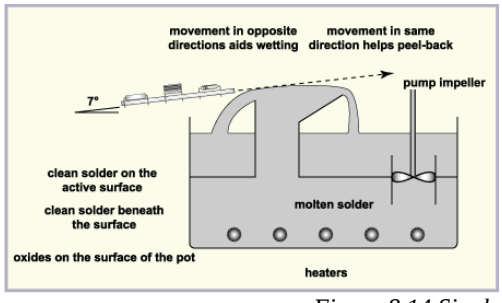


Figure 8.14 Single wave system [30]

- double wave systems (turbulent and laminar) as presented in Figure 8.15.

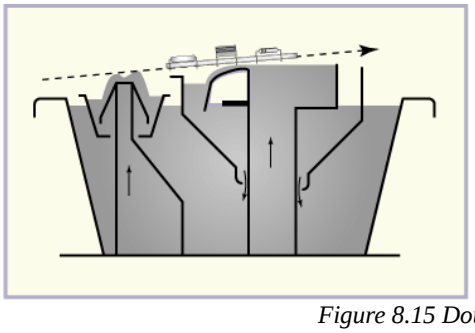


Figure 8.15 Double wave system [30]

Double wave systems are used when both SMT and THT components are soldered during the same wave soldering process. The turbulent wave is responsible for wetting the pads and leads with molten solder (easily penetrates narrow slits), while, the laminar wave is responsible for removal of excess solder.

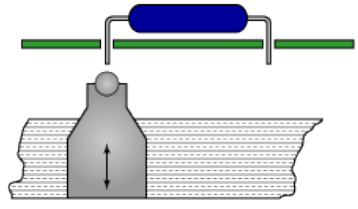
In-Line wave soldering system is presented in Figure 8.16 [33].

Figure 8.16 Wave soldering system [33]

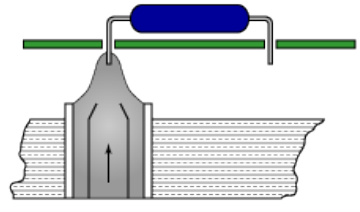
Selective soldering is a modification of wave soldering. Thanks to this method we can solder only chosen components.

We can distinguish:

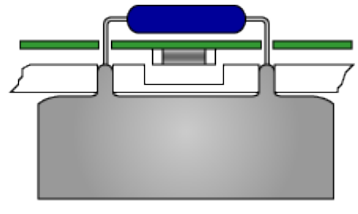
- pin transfer method [30],



- solder fountain [30],



- mini-wave method [30].



9. Defects of solder joints

The quality of solder joints depends on:

- wetting of the substrate by the solder,
- flux activity during soldering process,
- pad coating and termination coating,
- stencil printing,
- reflow profile (reflow soldering),
- wave shape (wave soldering),
- contaminations,
- pick and place process,
- other parameters of soldering process.

The standard ANSI/IPC-A-610 entitled “Acceptability of Electronic Assemblies” provides a division of electronic and electric equipment as follows:

- Class I :

Consumer products (includes TV sets, toys, entertainment electronics and non-critical consumer or industrial control devices),

- Class II:

General industrial (includes computers, telecommunication equipment, sophisticated business machines, instruments and certain non-critical military applications),

- Class III:

High reliability (includes life support items).

The standard provides a division of quality levels as follows:

- Preferred (close to perfect, desirable),
- Acceptable (will maintain reliability of the assembly),
- Rejectable (condition is insufficient to ensure reliability).

Faulty joints can be caused by improper process of soldering, improper materials or insufficient control of processes.

Typical defects of solder joints are:

- lack of connection,
- non-wetted surfaces,
- insufficient amount of solder in joint (concerns leads of through-hole devices),
- shadowing effect (concerns surface mount device),
- solder flags,
- shorts,

- solder balling,
- empty voids inside the joints,
- whiskers,
- etc.

9.1. Defects of reflow soldering

The most common defect of surface mount technology is lack of connection. It can be caused by non-wetting or dewetting. Non-wetting defect is presented in Figure 9.1, dewetting is presented in Figure 9.2.

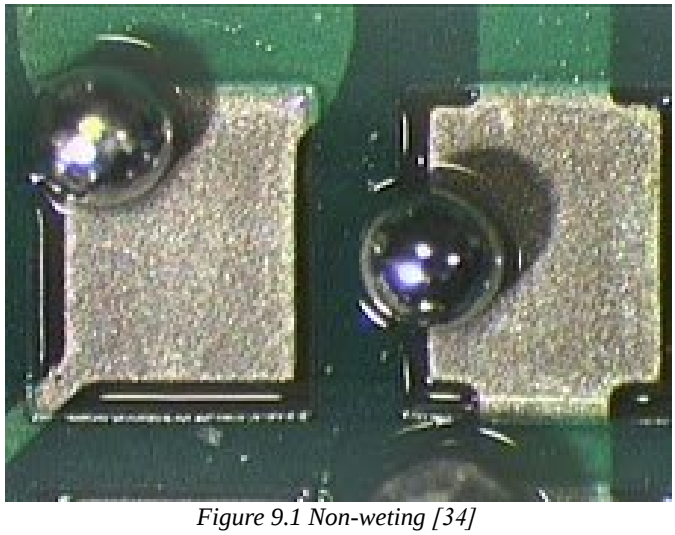


Figure 9.1 Non-weting [34]

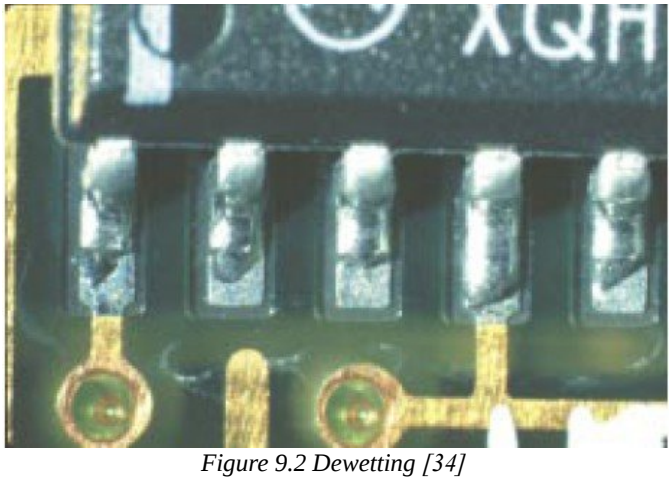
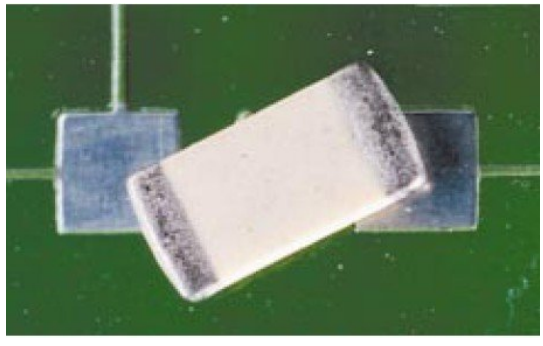


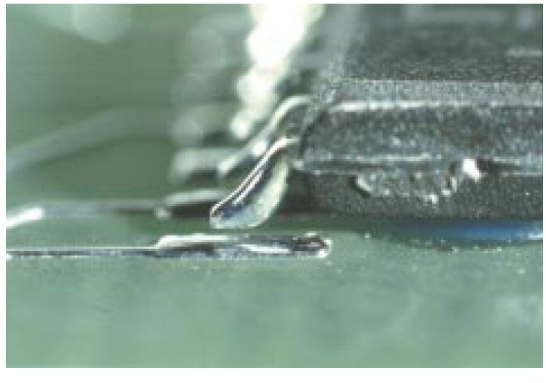
Figure 9.2 Dewetting [34]

Often encountered defects are assembly and placement defects such as:

- overhangs [34],



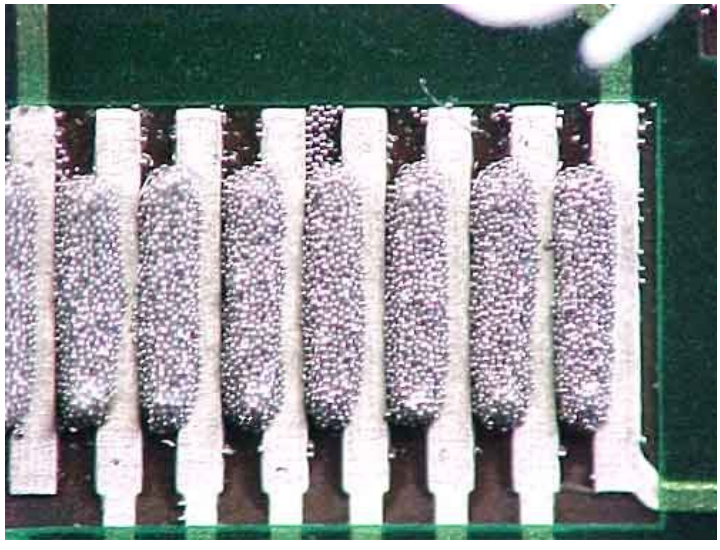
- misplaced leads and component movement. The end terminations lift the main body off the surface of the board and often out of the glue deposit [34].



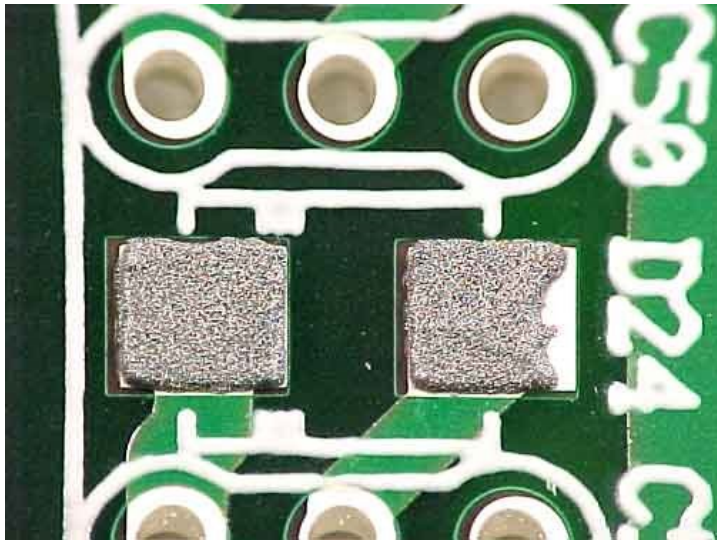
- cracked components. Cracking during placement is unusual today in the modern placement equipment. It is more likely to be seen in the older placement systems with mechanical centering [34] .

In case of reflow soldering the defects are often caused by defects from stencil printing and stencils such as:

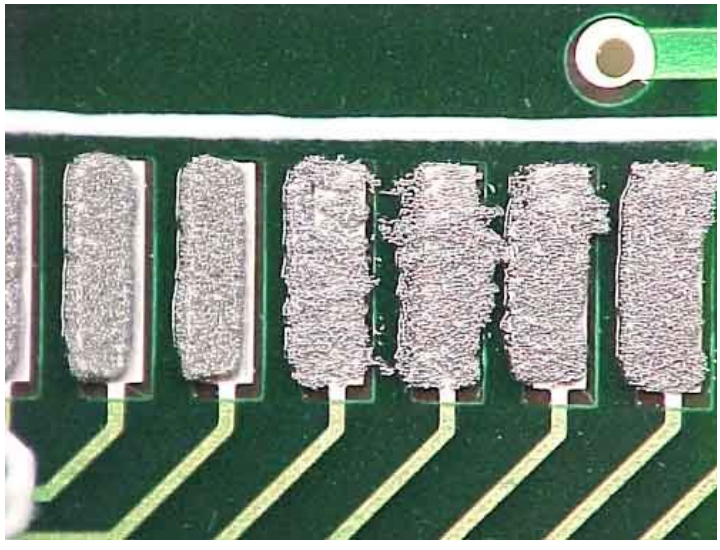
- buckles in the stencil,
- solder paste build up,
- an aperture blocked after laser cut,
- misalignment [35],



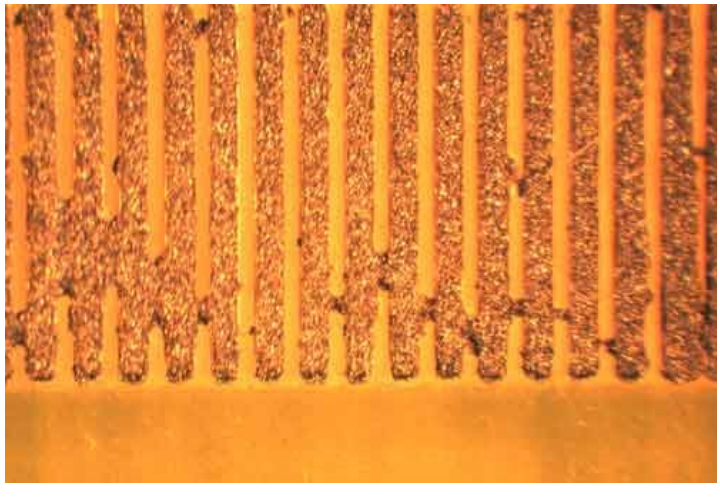
- incomplete print [35],



- smudges [36],



- shorts [35].



If a solder paste is deposited incorrectly shorts between solder pads and leads can occur. Such shorts are presented in Figure 9.3.

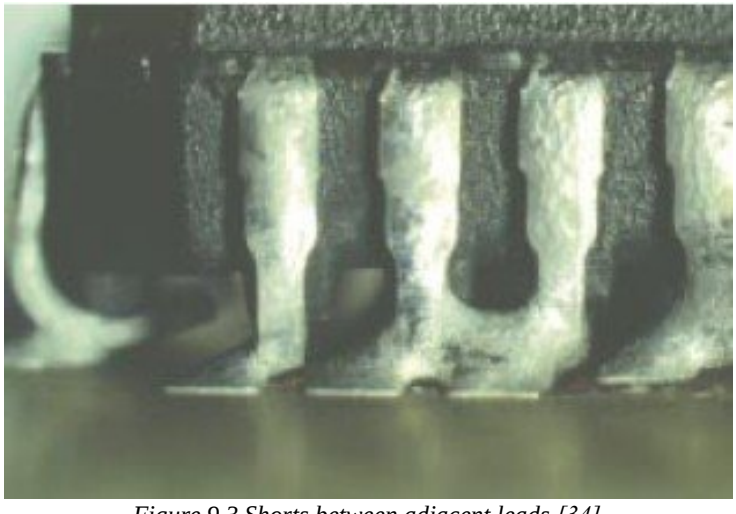


Figure 9.3 Shorts between adjacent leads [34]

Tombstone effect is a common defect in case of SMD components (resistors, capacitors). During reflow process one termination looses contact with the solder pad with the result that the component is in the vertical position. The tombstoning is presented in Figure 9.4.

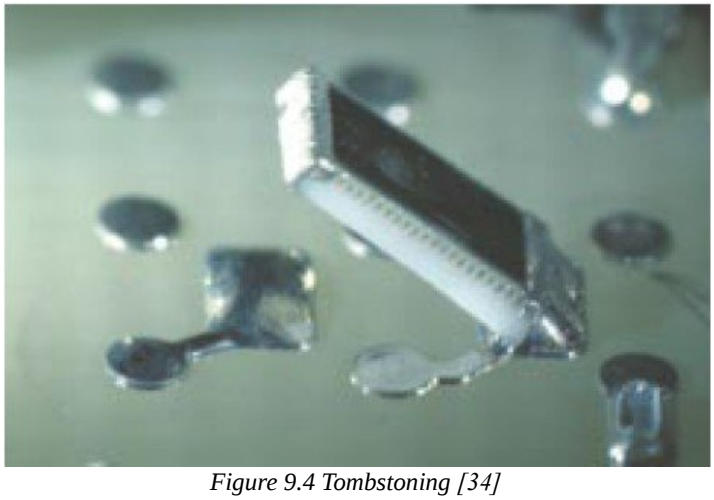


Figure 9.4 Tombstoning [34]

It can be caused by:

- differences in solderability of solder pads,
- improper size of solder pads,
- defects of the PCB design and temperature gradient along the component,

- improper amount of solder paste,
- improper parameters of soldering process.

Voids and blisters in solder joints (presented in Figure 9.5) can be the source of cracks. Especially when such solder joints are subjected to stresses caused by mechanical loading such as vibrations, mechanical shocks or temperature loading such as temperature cycles, temperature shocks. The cracks of solder joints are presented in Figure 9.6.

The voids and blisters may increase resistance of solder joints. The solder joint is considered as failed when voids and blisters exceed 25% of the surface of solder joint X-ray picture (as presented in Figure 9.7).

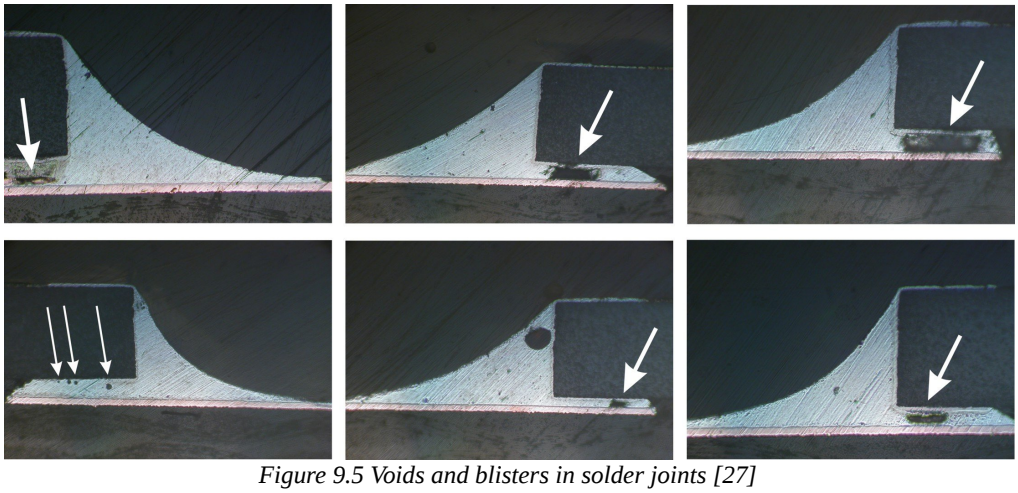


Figure 9.5 Voids and blisters in solder joints [27]

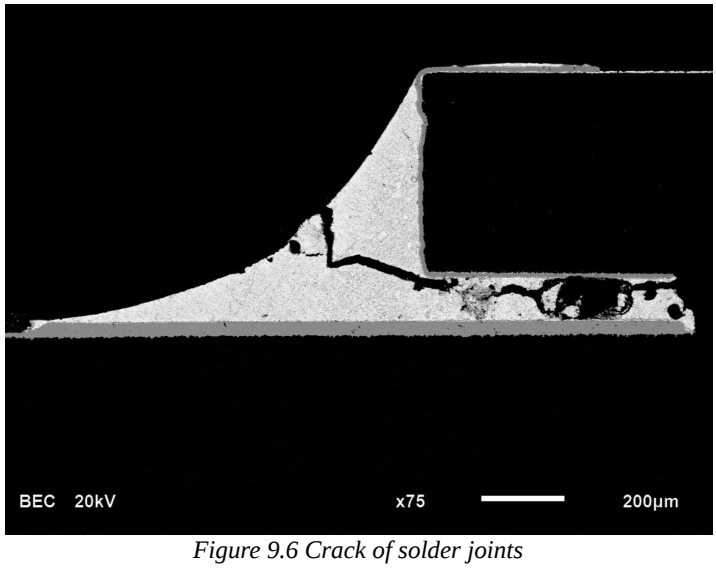


Figure 9.6 Crack of solder joints

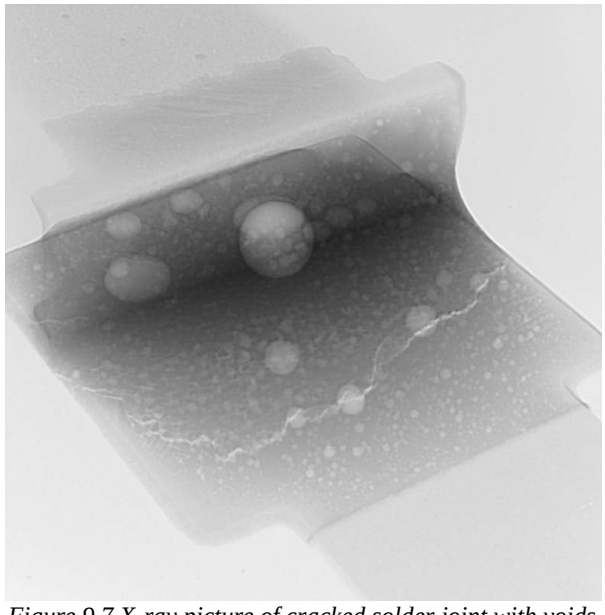


Figure 9.7 X-ray picture of cracked solder joint with voids

The solder balls attached directly to SMT components or under SMT components are typical defects in case of reflow soldering. This defect is called “solderballing”. Typical size of the balls varies from 50 to 500 μm depending on the cause. The main reasons are:

- improper composition of solder paste,
- excessive rate of heating.

An example of solder balling is presented in Figure 9.8.

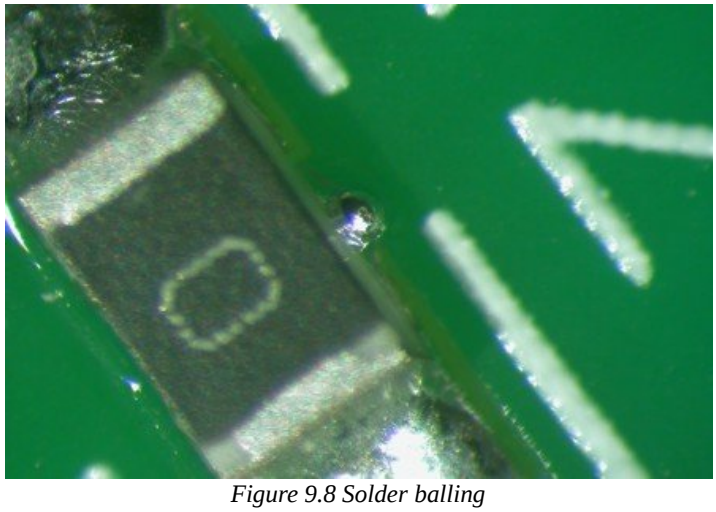


Figure 9.8 Solder balling

9.2. Defects of wave soldering

Typical problems of wave soldering are shadowing effect during wave soldering (SMD) and lack of full fill of holes (THD). The shadowing effect is presented in Figure 9.9. Skip of solder joint caused by the shadowing effect is presented in Figure 9.10. If solder pad exceeds the length of 1 mm, the curvature of solder alloy radius should be less than 2 mm, if the radius of curvature is less than 1 mm, both lead and solder pad (that exceeds the length of 0.5 mm) will be wetted with molten solder. In order to reduce the shadowing effect turbulent wave is applied.

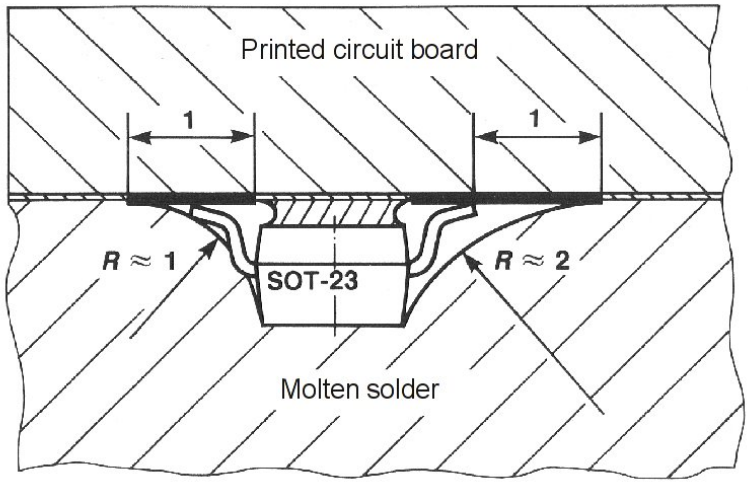


Figure 9.9 Shadowing effect [16]

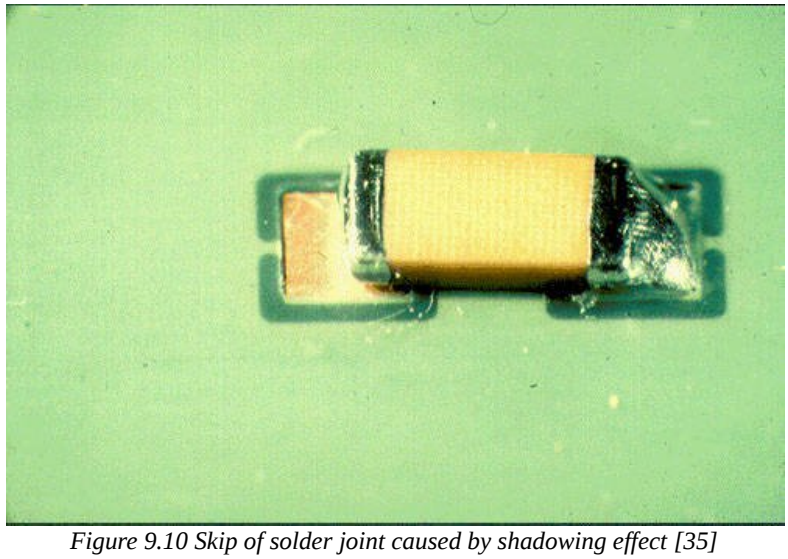


Figure 9.10 Skip of solder joint caused by shadowing effect [35]

Metalized holes are not filled with molten solder joint for:

- too little activity of flux,
- too high temperature in preheating zone,
- to short duration of contact with molten solder,
- irregular temperature distribution on printed circuit board.

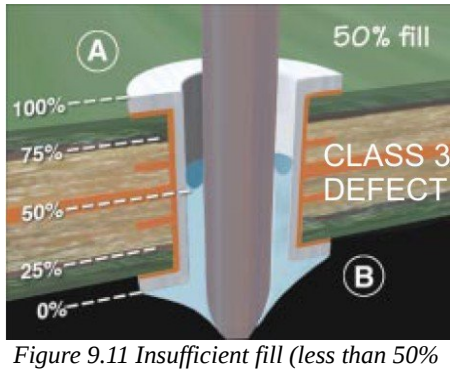
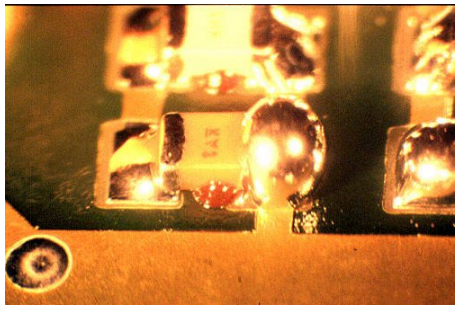


Figure 9.11 Insufficient fill (less than 50% according to IPC A-610 Standard)

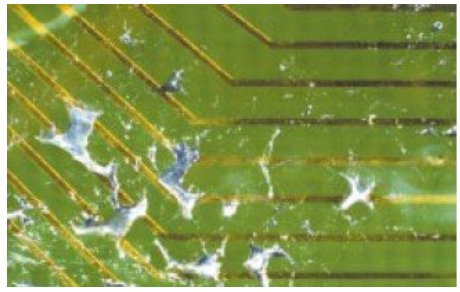
Other common wave soldering defects caused by improper process parameters are:

- incomplete joints [34],

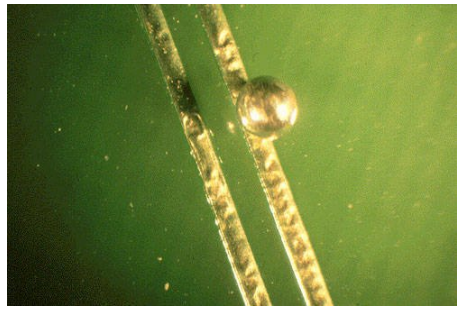
- bulbous joints [35],



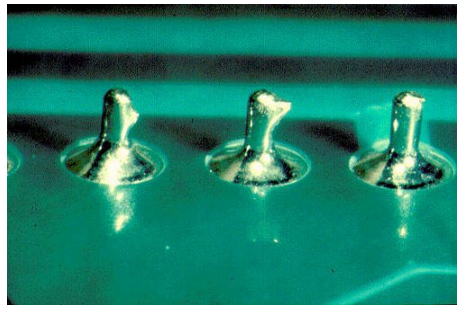
- solder webbing [34],



- solder balling [35],



- solder flags [35].



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